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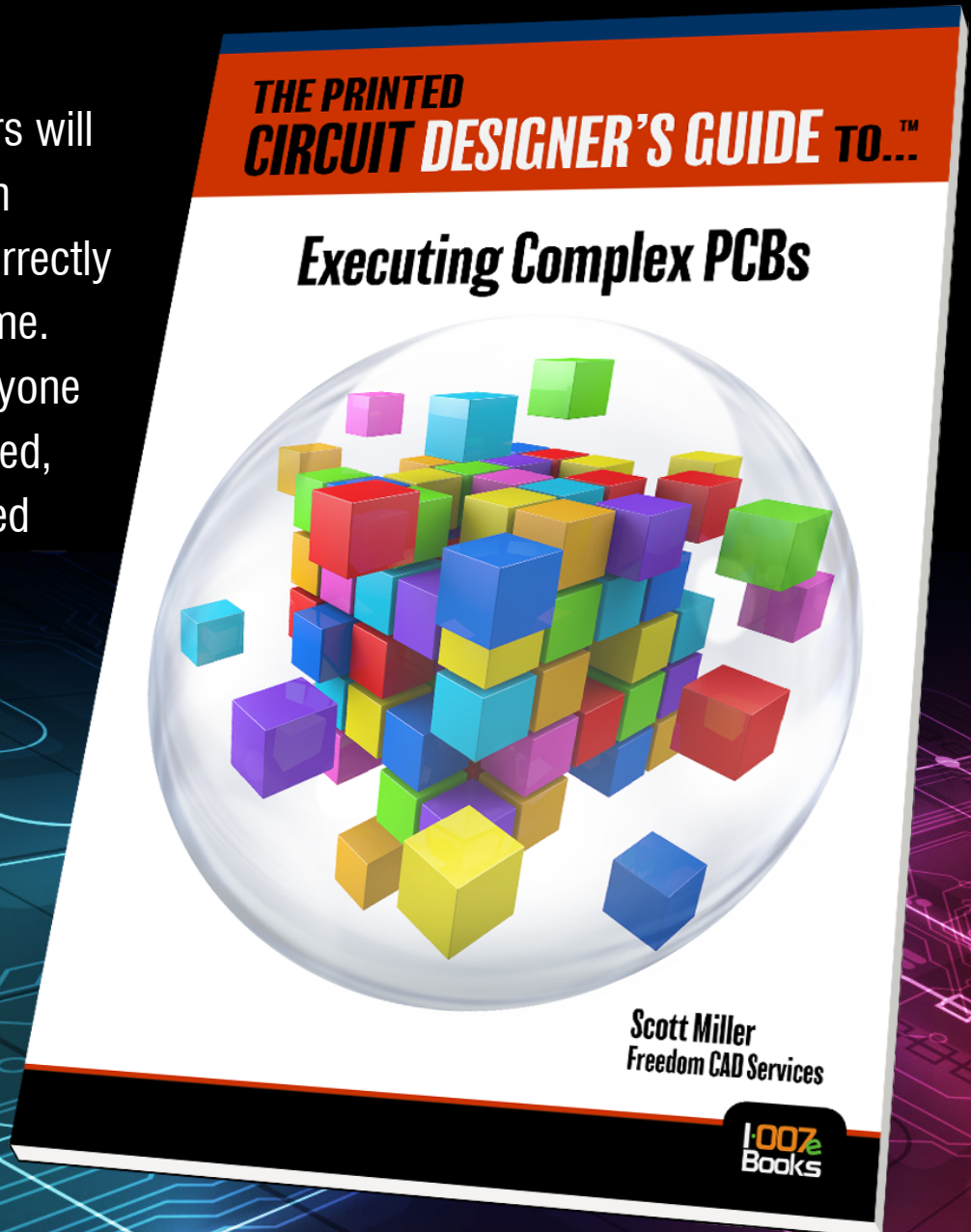
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Everything Starts With Design

Designers were once seen as little more than electronic techs. Now, many designers are starting to realize the power they wield over the whole electronics process. As you'll learn in this issue, there are plenty of little things that a designer can do to help make the board easier to fabricate and assemble, and even influence the profitability of the final product.



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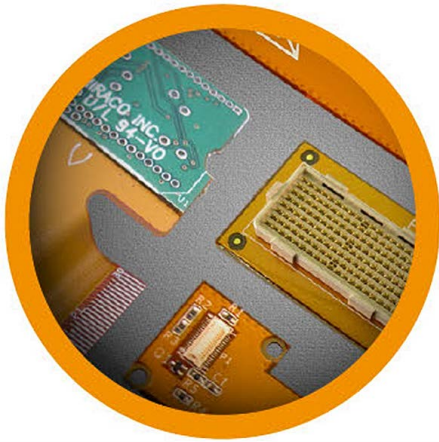
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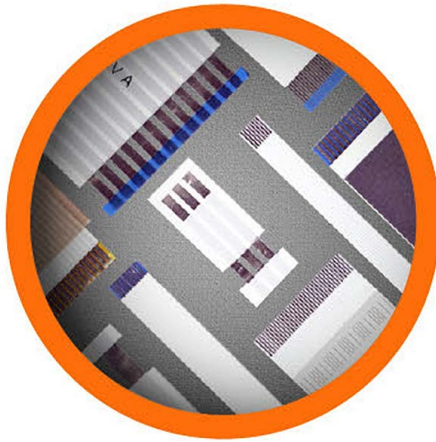
by Tim Haag



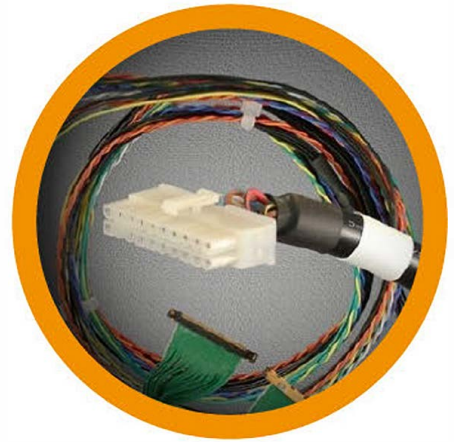
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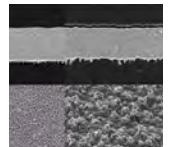
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IT-170GRA1

IT-170GRA1 Value Proposition

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- Best in class CAF performance
- Very attractive price to performance ratio
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Tg 180°C by DSC, low CTE

Applications

Server/Storage/Switch (10G, 40G)
Backplane, Telecom
Base station



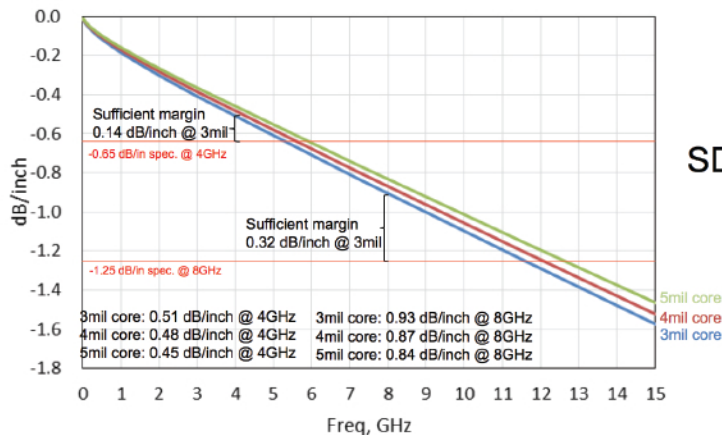
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Purley Platform Mid-Loss Solution – Hi Tg

General Properties

Items	Methods	IT-170GRA1
Tg (°C)	DSC	180
T-288 (w/ 1 Oz Cu, min)	TMA	60+
Td-5%(°C)	TGA 5% loss	380
CTE (%), 50-260°C	TMA	2.4
Peel strength (lb/inch)	1 oz	7.0
Water absorption	D-24/23	0.1
Dk: 2-10 GHz	Bereskin	3.96 – 3.99
Df: 2-10 GHz	Bereskin	0.0073 - 0.0075

IT-170GRA1 Insertion Loss



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Everything Starts With the Designer

The Shaughnessy Report
by Andy Shaughnessy, I-CONNECT007

Once upon a time in the not-too-distant past, PCB designers were the Rodney Dangerfields of the electronics industry. They didn't get no respect, and in some cases, not much of a salary either. But times have changed. Now, many

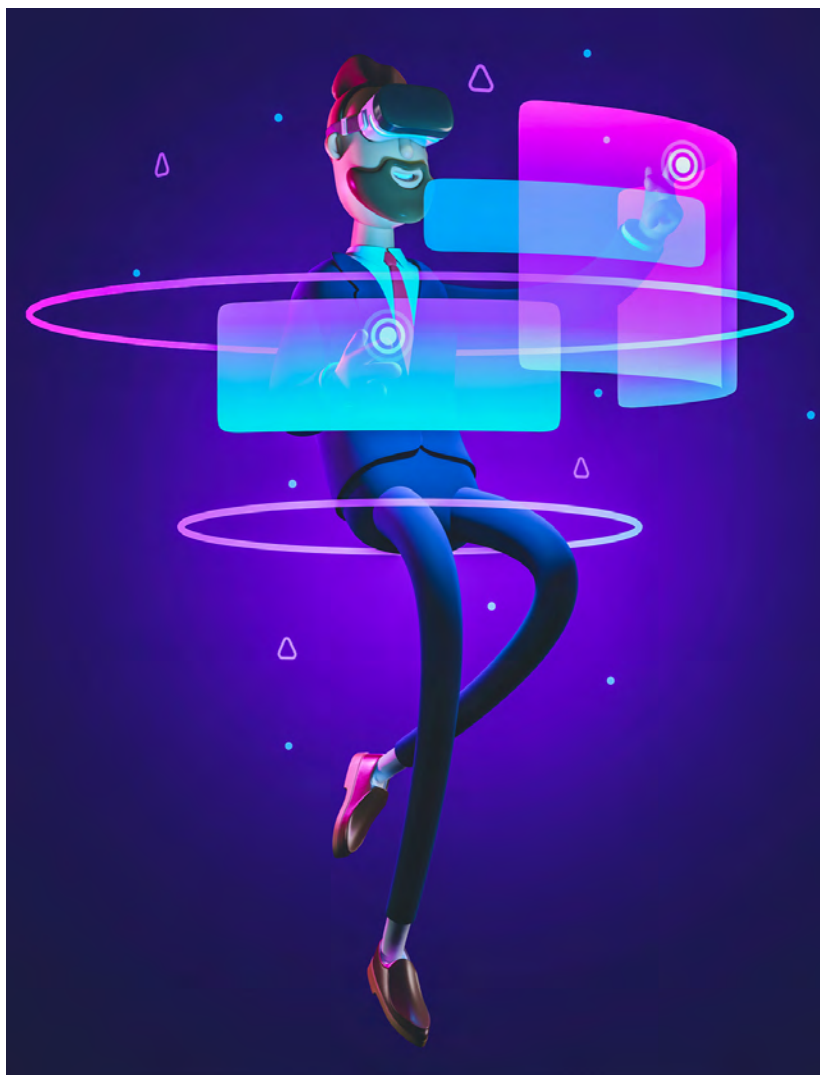
designers are starting to realize the power they wield over the whole electronics process.

The folks downstream in fabrication and assembly understood this sentiment long ago, usually expressing it as, "It's the designer's fault." But recently, a variety of manufacturers have told me, "Everything starts with design."

That's certainly a more positive spin! Everything does start with design—the positive outcomes as well as the negative. The designer can control much of the development of the PCB, and often the final product, with a little planning during the earliest part of the design cycle. It's a designer's responsibility to do everything possible to avoid getting that call from the CAM department at 5:30 p.m. on a Friday.

We surveyed our designer readers in preparation for this issue. Here's one of the more pertinent questions: What steps do you take to make the job easier for your fabrication and assembly providers? Here are a few of the replies:

- Communicate directly with them, especially if you want to try something new
- Follow proven design methodologies and rules



- Get feedback on previous builds to improve upcoming projects
- Try to insist that the fab house runs Valor DFM
- Minimize layer count
- Use the largest trace widths, via sizes, and clearances we can
- Don't use more demanding fab technology than absolutely necessary
- Plan your stackup with your fabricator
- Reduce the drill count
- Follow IPC standards

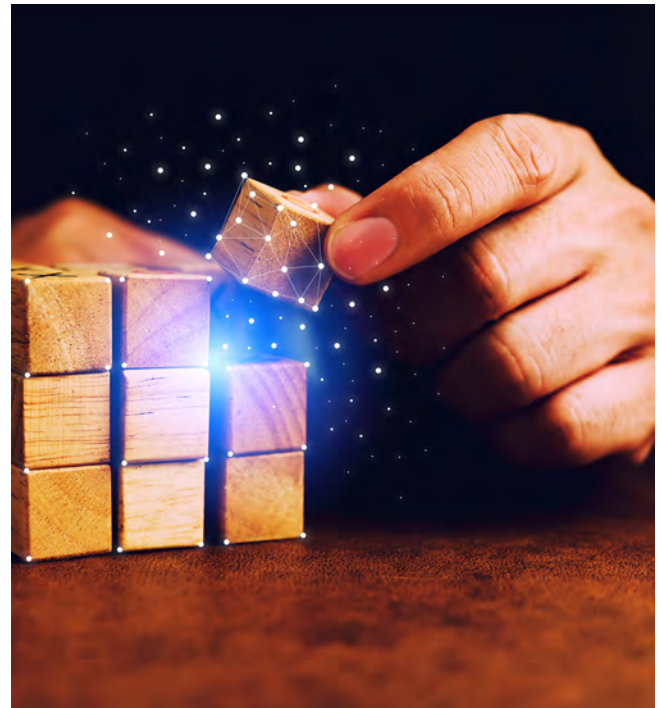
A lot of the replies were variations on these themes: Communicate. Don't throw your downstream partners any technological curve balls. Go big if at all possible, except for layer count. Follow IPC guidelines.

All of this might make us think that the days of throwing the design "over the wall" are just about over. But there are still flies in the proverbial oatmeal. We know that communication is still a big problem; many designers never speak to their fabricator until they get that Friday evening phone call. But many designers say that they have no earthly idea where their boards are going to be manufactured. They just design each board so that it can, hopefully, be fabricated anywhere.

As you'll see in this issue, there are plenty of little things that a designer can do to help make the board easier to fabricate and assemble, and even influence the profitability of the final product.

In our first feature, Prototron's Mark Thompson, CID+, explains why great fabrication jobs always start with solid design practices, and he lays out some of the things designers should—and should not—do to help make the design more manufacturable. Then, in an interview with our editorial team, Julie Ellis of TTM discusses some of the tips and tricks designers should adopt, especially if their boards are going to be built in Asia. As Julie says, you need to know your fabricator's capabilities or you could be up a creek without a paddle.

We also have an interview with Al Gaines, founder of HiGain Design Services. He takes "everything starts with design" one step fur-



ther: Everything starts with documentation, which Al describes as the most critical product that each designer can create. Next, Kelly Dack, an IPC CID designer instructor with EP-TAC, introduces us to his idea for the ultimate in DFX: Design for the Unknown, or DFU. Kelly also offers some advice for dealing with one of the newest cogs in the machine: the industrial designer.

Columnist Tim Haag explores the relationship between good PCB design processes and the recipe for a birthday cake; changing one ingredient can change the entire outcome! And we have a short interview that Nolan Johnson conducted with Mike Creedon of San Diego PCB Design. Mike discusses the need to select the appropriate type of laminate as early in the design process as possible.

Yes, everything starts with design. You may have already known that, but now your downstream partners do as well. We'll do everything we can to help you along the way.

See you next month! **DESIGN007**



Andy Shaughnessy is managing editor of *Design007 Magazine*. He has been covering PCB design for 19 years. He can be reached by clicking [here](#).

Fabrication Starts With **Solid** Design Practices

The Bare (Board) Truth

Feature Column by Mark Thompson, CID+, PROTOTRON CIRCUITS

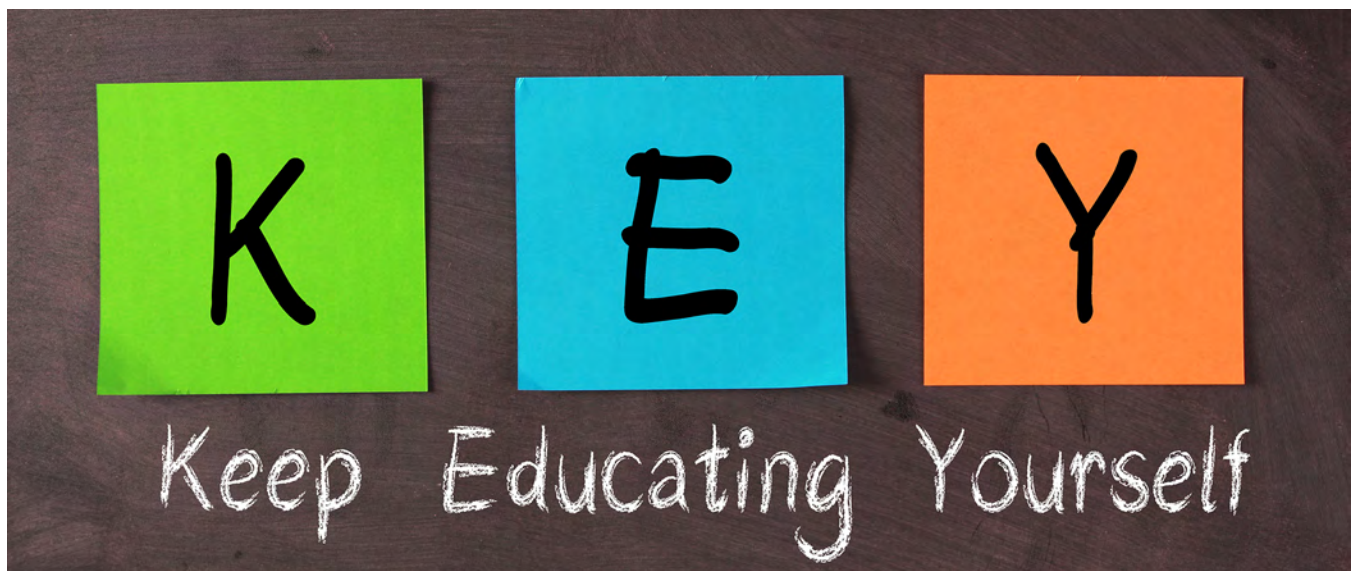
“All right! Don’t rush me. I’m a-thinking... and my head hurts.” —Yosemite Sam

It’s a fact: Great board design is the key to a great PCB. I’m even more certain of this after spending two days in a wonderful class presented by Rick Hartley titled “Control of Noise, EMI, and Signal Integrity in High-speed Circuits and PCBs.”

First, I would like to thank Rick for teaching his course. I thought I had a pretty decent grasp of controlled impedance and signal integrity, but the gaps in my knowledge base can fill the Grand Canyon. This class helped me see how important the design truly is not only for functionality but also for minimizing revisions and passing EMI testing the first time. I deal with incoming designs for a living, but I had no idea how many things you should consider when doing a board layout, from part placement and organization to via location.

I guess I am just accustomed to simply using my field solver and answering fabrication-related questions to make a PCB producible. I thought I knew it all, from effective Dk and Er to layer “nesting” based on the layer interfaces and prepreg selection for various controlled impedance structures. I assumed I knew what I needed to know from how the color and dielectric of a mask can affect controlled impedances to the use of ultra-thin dielectrics to increase inductance to pass EMI. Well, I was wrong!

How far we have come from the days of slower-speed designs; their edge rates didn’t matter very much because they were are basically lumped elements. Those old designs are nothing like today’s high-speed designs and all the bugaboos associated with distributed length line designs. Understanding the impact of nearby traces on controlled impedance lines and how magnetic fields work can make the



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difference between a successful design and a quagmire of self-created issues, such as common-mode emissions that can make or break passing EMI testing.

I even learned a few things about via filling with silver-epoxy or copper-epoxy for thermal applications. Remember, if you are using a via fill for conductivity, you are missing the point; the electromagnetic fields are generated around the barrel of the holes, not the material filling the hole. In some cases during Rick's presentation, I wanted to slap myself in the forehead and say, "I should have had a V-8!"

Remember, if you are using a via fill for conductivity, you are missing the point.

Rick showed one slide with four examples to be rated from least to most of radiated EMI. Fortunately, they are the same as a firing order in most four-cylinder combustion engines (1, 3, 4, 2) and pretty much everyone understood not to rout a trace over a split or a slot.

On many occasions during Rick's presentation, I began to make sense of some of the crazy things we have been asked as a fabricator over the years. Eight years ago, one customer asked us to mill a channel in a thick PCB using an end mill to make the corners as square as possible (not routed with a radii) and plate the trough and cap the whole structure with what appeared to be a wide plated "trace" running the entire length and width of the channel. At either end was a small hole where I was told they would inject a liquid. Then, I saw Rick's slide saying, "Apply a wave whose half wavelength is equal to distance X. We have a perfect balance and a true waveguide."

We were basically creating an acoustic waveguide through the Z-axis of a PCB. A 1995 article by L. Dwynn Lafleur and F. Douglas Shields of the Acoustical Society of America noted, "It is shown that certain combinations of material

properties can produce a mode, which in zero frequency limit, has plane-wave motion in the liquid." This is presumably why the customer was injecting liquid into the waveguide. Great stuff!

I did know a few things that Rick covered in his class, like routing longer differential pairs and clocks inside the PCB and keeping the shorter traces to the outer layers. But I only thought I knew why; when solving for impedances internally, the differential pairs and single-ended structures are more forgiving. The electromagnetic wave field is not completely contained in the substrate as with a stripline used internally where the EM field is contained within the substrate. This is at least partially due to the Dk of air over the trace on an outer layer.

Great Fabrication Starts With Great Design

Again, I remember when I was asked to review a design for a customer from the standpoint of manufacturability. It was an 18-layer board where all layers had impedances. The layers had reference planes like a checkerboard above and below signals alternating back and forth on every layer.

From a pure design perspective, it was a work of art. But could it be produced? It turned out that all the traces were laid out with the same trace width and different spaces (for multiple differential pair scenarios of 90, 100, and 120 ohms) and ground separations on every layer. In conjunction with that, all of the copper pour used the same trace width they had used for the signals—both single-ended and differential pairs.

There were five different scenarios with the same trace width, making it virtually impossible to tweak any of the signal traces, and all of this had to be done through changes to dielectrics and material type. I spent the better part of a day looking at what could be done and came up with a specific dielectric and material combination to make it all work without having to change the trace widths at CAM. With five different scenarios, that would have been a nightmare.

Along with the stackup and material type, I said that the design would benefit from chang-

ing the trace width size from five different scenarios to five different trace widths by one-tenth or one-hundredth of a mil. This was with the knowledge that the slight variations could not be resolved in fabrication, but this would allow a CAM operator to resize the unique trace widths without affecting the other scenarios. Once everything was said and done, I presented the material type and dielectrics to the customer, who promptly said, “No, that material won’t work for us.”

The best-laid plans do not always work in fabrication. That part was eventually redesigned to reduce the layer count, opening up the possibilities for dielectric changes, high-speed materials, and reduced impedance scenarios. It also had five trace widths from the same size to one-tenth or one-hundredth of a mil for us to pick them out for resizing to meet the desired impedances.

After reading all of this, you’re probably thinking, “What is your point?”

I cannot overemphasize the need to check with your fabricator before starting layout, from the proper ϵ_r of the material you are using to modeling the impedances with a true field solver and questions about the mask dielectrics and ϵ_r data associated with the mask.

Just 10 years ago with 0.008”/0.008” spaces and traces, it was no big deal to have a mil or two of mask over the trace. But with today’s geometries of 0.003”/0.003”, that extra mil of mask will definitely affect the impedances. Before you lay out a part that may have to change (which nobody likes), consult your chosen fabricator.

“Helping” Your Customer

This is also known as “How did we get into this mess?” Let me give you an example.

Let’s say the customer provides internal plane relief pads that are undersized based on your capabilities. But you say, “It is only a four-layer. Starting with 0.006” clearances from the edge of the non-drill-compensated plated hole will leave us with approximately 0.004”.” But you are able to pull it off for that job.

The customer thinks all the designs can use that same relief size, so they send a 14-layer

with the same relief sizes. This time, the person previewing the job says this won’t fly and asks the customer to increase the relief sizes. Then, the customer is NOT happy, because they do not have the time to lay out the entire job again, saying, “Well, you did it on the four-layer last week.” Now, you have an upset customer solely because you were trying to do them a favor on the four-layer, which you were not when you suggested that they could live with the undersized reliefs.

The customer has a 14-layer and has used the same insufficient relief sizes. This is why we have capability minimums that should not be busted, even on the four-layer, unless the customer is made aware that they are risking internal misregistration issues and that you can do this one time. Do not make it the norm.

These types of conversations should take place between a pre-engineering person and the designer, not a manufacturing person or a salesperson. You are doing the customer a disservice by “pulling something off” when the risks of doing so should be clearly described to the customer. Don’t be that fabricator!

Another issue we should discuss is drill files. It seems that fairly often, the NC drill file comes in with a totally different numerical format than the artwork. Sometimes, blind vias, buried vias, and through-holes all arrive with different numerical formats, leaving the preview person to figure out what the format should be.

**It seems that fairly often,
the NC drill file comes in with
a totally different numerical
format than the artwork.**

It’s true that looking at the NC drill file coordinates can help determine whether the format should be leading zero suppression, trailing zero suppression, or no zero suppression. Some come in as a mix of metric for tools and

imperial for dimensions and vice versa, and the format is frequently different from that of the image data. Presumably, if you have a specific format for the image data, the NC drill file should have the same numeric tolerance, so mixing numeric data formats should be avoided. The most typical NC drill format is set to “inch” for both the tool size and the dimensions. The most used formats are 2:4 (for positional accuracy) and trailing zero suppression.

Now that I have gotten off my soapbox, let me end by saying that a good CAM operator can always figure out the proper numerical format to match the NC drill drawing. But do yourself a favor by at least making them consistent. Don’t make the non-plated tool file one format and the plated holes another. Likewise,

do not make the blind vias, buried vias, and through-holes all different numerical formats.

As Rick often says, “Don’t take things for granted and don’t believe everything you read until you have proved them for yourself empirically or by making mistakes.”

Thanks again, and as always, feel free to contact me any time. **DESIGN007**



Mark Thompson is in engineering support at Prototron Circuits. To read past columns or contact Thompson, [click here](#). Thompson is also the author of *The Printed Circuit Designer's Guide to... Producing the Perfect Data Package*. Visit www.I-007eBooks.com to download this book and other free, educational titles.

Researchers Identify New 2D Insulators With Ferromagnetic Properties

Collaborating scientists at the U.S. Department of Energy’s Ames Laboratory, Brookhaven National Laboratory, and Princeton University have discovered a new layered ferromagnetic semiconductor, a rare type of material that holds great promise for next-generation electronic technologies. The researchers discovered ferromagnetism in a vanadium-iodine semiconductor, a material which has long been known but ignored.

“Being able to exfoliate these materials down into 2D layers gives us new opportunities to find unusual properties that are potentially useful to electronic technolo-

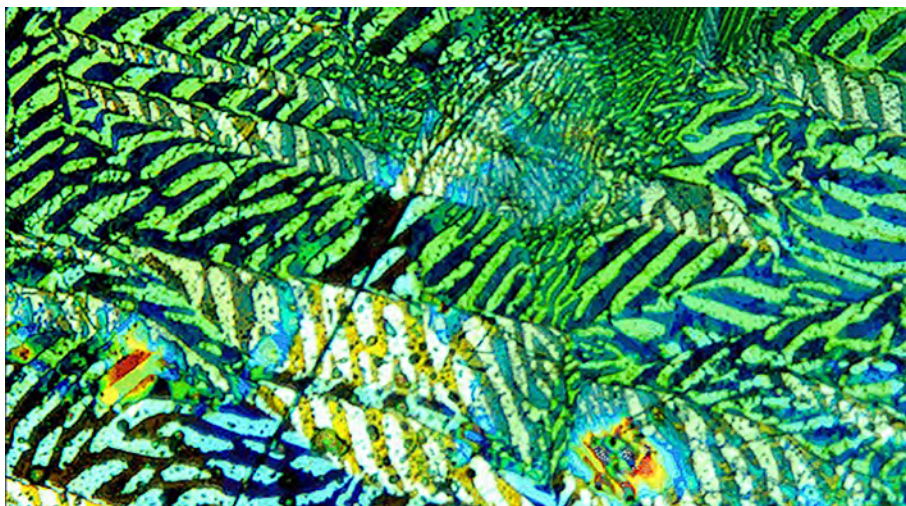
gy advances,” said Tai Kong, a postdoctoral researcher in the lab of Robert J. Cava, the Russell Wellman Moore Professor of Chemistry at Princeton University. “It’s sort of like getting a new shape of Lego bricks. The more unique pieces you have, the cooler the stuff you can build.”

The advantage of ferromagnetism in a semiconductor is that electronic properties become spin-dependent. Electrons align their spins along internal magnetization.

“This creates an additional control knob to manipulate currents flowing through a semiconductor by manipulating magnetization, either by changing the magnetic field

or by other more complex means, while the amount of current that can be carried may be controlled by doping (adding small amount of other materials),” said Ames Laboratory Scientist Ruslan Prozorov. “These additional ways to control behavior and the potential to discover novel effects are the reason for such high interest in finding insulators and semiconductors that are also ferromagnets.”

(Source: Princeton University)



“Mark does an outstanding job detailing what needs to be included in the handoff from designer to fabricator. This book should be required reading for every designer.”



Douglas Brooks, Ph.D.
BS/MS EE

Most of the design data packages that a fabricator receives contain inaccurate or incomplete data.

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Design Is a Pivotal Piece of the Puzzle

Feature by the I-Connect007 Editorial Team

As a field applications engineer at TTM Technologies, which has fabrication and manufacturing locations around the world, Julie Ellis sees a wide variety of customer design requirements. In this interview with the I-Connect007 Editorial Team, Julie explains how PCB designers can influence the development of the PCB. She shares a variety of tips and tricks that designers can implement early in the design process to help optimize fabrication and assembly later on and keep small issues from becoming big problems downstream.

Andy Shaughnessy: Julie, with your job you have a pretty circumspect view of design and manufacturing. Can you start by giving us an idea about your job and some of the designs that you see crossing your desk?

Julie Ellis: My main task is to support customers' designs for manufacturability by understanding their requirements and providing

stack-ups and design guidelines for rigid circuit boards that are within TTM fabrication capabilities and process tolerances. I also help customers understand how fabrication processes affect capabilities, so they accept design modifications that assist in manufacturing.

The work I see coming across my desk includes components for EV charging and power conversion, Lidar, radar, back-up and industrial scanning cameras, ultrasound, defibrillators, and glucose monitoring. They require stack-ups ranging from four-layer heavy copper boards to 32 layers with three lamination cycles and mechanical blind holes and advanced HDI, which I define as 0.4-mm pitch BGAs and smaller.

Oftentimes, I'm trying to help customers design products that can also easily be transferred over to Asia and run on mass volume production lines without any advanced requirements that add cost. I work to ensure that prototypes fabricated here in North America are already designed with pre-approved stack-ups to run without modification at the final production

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Julie Ellis

volume site or sites. TTM calls this Seamless Global Transfer, and it works best when implemented in the planning stages of a new design.

I also review designs for cost savings. For example, in Asia, materials are 40 to 50% of a fabricator's cost, compared to less than 20% in the United States. When we get into high-volume manufacturing, optimizing material utilization can save a customer several percent on the final assembly if we can keep a lowered cost on the PCB by planning the PCB dimensions to fit very well on a fabrication panel. If the circuit board is small, TTM often works with our customers to calculate the best multiple-up array with rails for assembly that can still fit optimally on the fabrication panel. The most common fab panel size is 18" x 24", but we also mass-produce 21" x 24" panels at many sites.

Shaughnessy: Sometimes, I get the feeling that the designers don't realize how much control they have over the final product. What are some of the common errors that you see coming in that you wish that you could just tell the designer, "If you just did this...?"

Ellis: If you just...came to me for your stack-up and design rules first, I wouldn't have to tell you that nobody can fabricate this design in mass production. I request of my custom-

ers that they come to me at initial startup of a product before they even bother to route any circuitry, because designs get so complicated that it's very challenging for them to go back and make changes if they've violated standard fabrication design guidelines. It's really stressful to explain to an engineer why his design isn't suitable for mass production, so I prefer to avoid that like the plague.

The information I request from the designer includes:

- Initial prototype and final volume production region/sites
- Material type
- Overall thickness
- Layer count
- Layer copper thicknesses
- Layer designations (signal, plane, mixed)
- Smallest component, connector, or BGA pitch
- Smallest expected lines/spaces for plated and non-plated layers
- Drill structures and traces required for fan-out
- Controlled impedance requirements
- Special requirements (require non-standard materials, additional processes, or tighter tolerances)
 - High speed, low Df materials
 - Plugged or filled vias-in-pad (VIPPO)
 - Back-drills
 - High voltage or current
 - Optical routing
 - Dual finish plating
 - Edge plating
 - Castellations
 - Cavities
 - Thermal management
 - Press-fit holes

I always ask what the minimum BGA pitch is if there's a BGA, because the most difficult component establishes the level of technical capability required. And I can provide basic design guidelines per device pitch. With a 0.4-mm pitch BGA, if a customer is trying to run one trace between the pads on internal layers, those traces and spaces can only be 2.36

mil because of the small distance between the pads. Most fabricators don't have the etching capability to do that, and we have to be careful to follow the design guidelines of the fabricators that can support the small lines.

Shaughnessy: What sort of mistakes do you see when the design moves to volume production overseas?

Ellis: Here's a recent list of common design errors for jobs going into mass production:

- Multiple semiconductor reference designs using a 6-mil drill and 10-mil or 11-mil pad as a through-hole to route a 0.5-mm pitch BGA. A multi-row 0.5mm pitch BGA requires layers of microvias, because we only use mechanical drills, not lasers, for through-holes, and mechanical drills have larger tolerances than laser drills. So with a minimum standard pad of 16mil (= 8-mil drill + 8-mil to maintain Class 2 annular ring), mechanical drill pads are too large for fine-pitch BGA routing. And laser pads, at laser drill diameter plus min 6-mil = 10-mil min, are way too small for mechanical drills.
- Designs that are prototyped in North America with 6-mil drills transferring to China, where the vast majority of fabricators can handle a minimum 8-mil drill size. Check your fabricator's min drill size before routing.
- A circuit board was designed, fabbed, and assembled before anyone realized there were no access pads for functional or in-circuit test anywhere.
- A 6-layer stack-up with 6-mil drills on 10-mil pads going from L1 to L4 and L6 – L3 with dielectrics that are too thick to use stacked microvias and maintain a max aspect ratio of 0.75:1.
- Another semiconductor reference design had 3mil lines and spaces on an outer through-hole layer with VIPPO—via-in-pad (filled) and plated over—which requires an extra plating process, which increases the copper thickness before etch.

Shaughnessy: In the designers' defense, they would probably say, "We don't know where it's going to be built or whether it's going to be built in Asia." Is it up to them to try and find out where it's going to be built, if it's going to volume, and then get in touch with those manufacturers?

Ellis: Absolutely. In the last year, I've had to convert several designs that could have been simple through-hole designs, but they worked with North American suppliers who must have said, "Yes, we can drill a 5-mil mechanical drill with a 10-mil pad on a 0.62" board." That is greater than 10:1 aspect ratio; it's using a 5-mil bit that's not even common for prototype in America, much less in mass production over in China. The poor customers think that they can use very small pads with small drills on through-holes and transfer it to China, but nobody in China can do it.

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I may seem overly regimented, but I tell my customers that I'm an equal opportunity—and conservative—designer. With the rules I give them for standard design guidelines, if they're using a halfway decent supplier, they will be able to fabricate their design at many locations, including our competitors. Sometimes, you give away information that's going to help somebody else. But if you don't train your designers correctly in the first place, you're going to be battling designs that you cornered into one factory, and then it's going to be hard for everybody to maneuver, move forward, and grow into higher volumes. I recommend fair design rules for standard production, design

permitting, hoping that we end up booking the business. And when the standard rules are too tight to meet requirements, then we may loosen the rules to more advanced capabilities, which increase cost.

Shaughnessy: What are some of the guidelines that you give these designers?

Ellis: We provide design presentations for different requirements, including BGA and DFM design guidelines and technology capabilities for each TTM fab site. After I've reviewed all the design inputs for specific projects, the site-approved information I provided the customer includes:

- Stack-up graphic showing Cu layers, dielectrics, and drill structures
- Controlled impedance table, if required
- Mechanical and laser via hole min drill/pad diameters
- Min. lines/spaces for plated/unplated layers based on starting Cu foil thickness
- Design rules for special requirements, as necessary

Nolan Johnson: You're saying that you start with a qualification process to figure out what that design team's intent is with the board. How often do you find that they don't know, or are they mostly clear on that by the time they come to you?

Ellis: Approximately 80% of my work is with ongoing customers that I have a good relationship with, so I'm their first call for the stack-up, DFM guidelines, and sometimes to help with best PCB or array dimensions for panel optimization. Other customers mostly know where their business is going.

We support a lot of new development customers, so if one happens to be in the electric vehicle or medical space, it's a fair assumption that their PCB assemblies will eventually be manufactured somewhere in a high-volume region offshore. When I confirm Asia production intent on a new stack-up, I verify it with TTM China before sending it for customer review. Sometimes,

though, engineers need to test their electronic design. They're in a hurry, and they're very limited for space, so they'll use the prototype guidelines to quickly check functionality. And other designs are limited quantity test boards that will never go into full production.

Johnson: For the 20% of your customers that are new to you, do they tend to be as well prepared?

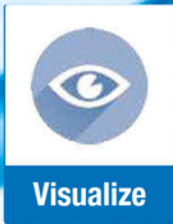
Ellis: Not necessarily, although a lot of new "customers" are actually familiar friends who moved from a previous customer. Most designers I work with already have some experience working with a fabricator, and the ones who haven't are normally glad to have the opportunity to learn.

Dan Feinberg: The customer can come to you for the entire package and get assistance, ideas, or recommendations regarding help with the initial part of the design.

Ellis: Yes. TTM has a design center in Stafford, Connecticut, where we can provide new electronic designs, redesigns, PCB layout, and electro-mechanical designs. Our Anaren division designs and manufactures high-frequency RF and microwave microelectronics, components, and assemblies for the space, defense, and telecom sectors. Our EMS sites in China do full turn-key PCB assemblies and box-builds. We also work with a lot of good design bureaus and can provide referrals to reputable outside resources for work we don't do.

Feinberg: Regarding designers working with others in expanding collaboration, what's happening with the designers working with the suppliers? I know that it didn't used to be the case, but it has become more of the case over the last number of years. For example, if a dry-film supplier comes up with a way to do lines and spaces with straight sidewalls with 0.5-mm lines and spaces, would you then go to a photoresist supplier in today's and work with them to discern if they can develop the material that would be congruent with your design?

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Ellis: No, probably not. TTM has over 30,000 employees with over 2,000 engineers, so there are other people responsible for looking at new technologies and implementing them globally. That's out of my wheelhouse, and I wouldn't have time to pursue it.

Happy Holden: Do OEMs come to you, saying, "We need this technology developed," or do you routinely have a roadmap that goes out a couple of years that you show good customers?

Ellis: I think both, because they're intertwined. Customers continually push TTM for new product development, which causes us to always increase our technology at our sites. Customers come to us with new technologies that they're looking for, and often, they're driven by the automotive sector, which is running the full gamut from HDI autopilot controllers to thick copper high-voltage applications. TTM executives plan future roadmaps to justify capital equipment expenditures needed to achieve those capabilities. We'll go out of business if we don't keep up with technology, and our technology is improving so rapidly that I can barely keep up with the changes by site.

We'll go out of business if we don't keep up with technology, and our technology is improving so rapidly that I can barely keep up with the changes by site.

Barry Matties: That's not terribly surprising because cars are increasingly becoming computers with wheels.

Ellis: Right, our cars are becoming entertainment and communication command centers.

Matties: You're in a unique position because you work with so many different designers. Is

there a difference in approach between the old guard and the new?

Ellis: It depends on personality. Some people naturally have curmudgeon personalities and want to do it their way or the highway, but usually, engineers are big learners. From my perspective, 95% of the people that I work with are amenable to looking at the best ways to optimize their circuits. For the most part, young engineers are glad to receive any advice that we give them for a roadmap to a good project.

Matties: Are their skillsets different than those of a 40-year veteran? I hear what you're saying that they're seeking knowledge, but I'm just curious if their approach or ideas are different.

Ellis: That's a really good question, and, again, it depends on personality and also company culture. Generally, younger designers are so excited about new designs and problem-solving, so they're fun to work with. Experienced veterans, on the other hand, can be vast sources of knowledge who expand my horizons through our discussions and design analyses. But I've also encountered companies that don't want their engineers to waste their time talking to suppliers, and that culture breeds Wizard of Oz designers who create impossible designs behind their curtains.

Matties: You said that about 80% of your customers are repeat customers, so it seems to me that they could streamline the process because they have these parameters from their historical dealings with you, or is that not the case?

Ellis: Yes, it is the case. For a customer's stack-ups and design guidelines, circuit modules are often copied from one design to the next. When other requirements on the new part don't change too much, we can modify an existing stack-up slightly and keep the original design guidelines for the new part. Maintaining history on designs is extremely time-efficient, and I love it when customers give me an old part number for reference on a new similar design so I don't have to reinvent the wheel on



the stack-up and design rules. We can also review the technical queries that came up during CAM on the old part and get them corrected on the new part, so we reduce the Q&A time delay on the new fab.

Very few of our customers can pay attention to the design rules enough to do their own panelization. I have a couple who do, but it would be great if customers were more aware of that. I think everybody gets confused because different sites and regions have varying requirements for the keep-outs required around the fabrication panels for tooling holes, and nobody is sure what width rails an assembler needs on the array to run through production. It's easiest if the PCB designer, fabricator, and assembler work together to get the rules for assembly, and then let the fabricator optimize the array on their production panel.

Matties: Right, because this thought up front can help drive cost out in the tail end.

Ellis: It does. Recently, I worked on cost-reduction of a North America production part moving to China. By reducing the rail widths on all four sides of the customer-designed array, I was able to increase panel utilization and reduce the unit cost 7.9%.

Matties: And when you're talking about 500,000 parts, that can add up quickly. You said that early collaboration is commonly offered as advice. What other advice would you give a designer who is seeking the most successful design and manufacturing experience?

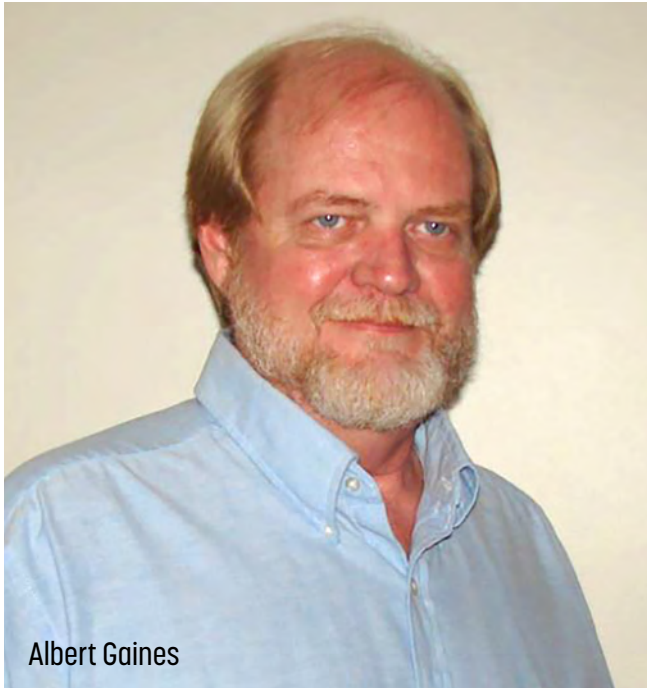
Ellis: Talk to your fabricator and assembler and follow the KISS (Keep It Super Simple) principle. From the user's point of view, if something goes wrong and they have to troubleshoot or fix something, a complicated, difficult-to-build design will also be difficult to take apart, repair or rework. Think of your whole system from the outside in, and then start building from the inside out, thinking of the bigger pieces that follow.

Matties: I appreciate your time, Julie. Thank you.

Ellis: Thank you. Everyone had interesting questions.

Shaughnessy: That was fantastic. Thanks a lot.

DESIGN007



Albert Gaines

Albert Gaines: Design All Comes Down to Documentation

Feature Interview by Andy Shaughnessy I-CONNECT007

During SMTA Atlanta, I spoke with Albert Gaines of HiGain Design. We discussed Albert's belief that everything starts with design and that too many engineers and designers focus solely on the final board at the expense of the documentation, which is a designer's most important product. Do you consider your documentation to be a critical product?

Andy Shaughnessy: Albert, you are the founder, chief cook, and bottle-washer for HiGain Design. A minute ago, we were talking about how everything in electronics manufacturing really starts with design. You had an interesting point about some things that designers and design engineers sometimes neglect to consider early in the cycle.

Albert Gaines: I've been doing board layout since '81, and I came through the drafting side of it. Documentation was our product. I think most engineers today lose the concept of the fact that the final product is not the prototype. They finally have it working, but they think they're through. But their product is documentation—the Gerber package, ODB++ package,

testability, assembly drawings, and all of the firmware. That documentation and traceability of that documentation is their product—not what's sitting in the test lab.

Shaughnessy: How did we get to this point? I'm sure that there are people who have been doing this for 30 years and have never looked at the documentation as their final product.

Gaines: A lot has changed over the years because we've had a shift to where more EEs are doing more board layout, and we don't have documentation departments in companies. Everybody is running freelance in their own cubicles. Nobody is enforcing what the documentation has to be. Ultimately, you end up with a board shop or an assembly house with a big void, wondering, "Am I going to get this data, the IPC-356 netlist, or the bare testing of the board? Or am I going to get an ODB++ for pick-and-place? What am I going to get? Do we have to recreate it after the fact?"

Shaughnessy: We always joke about how the designers get blamed for everything, but this sounds like one of the things that designers need to be aware of; it's more about the documentation than anything else.

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Gaines: Yes. It would be very good for each designer to have a checklist beside their desk when they're getting ready to finish a product, detailing what they need to do—not just generate Gerbers and NC drill files and send it over the fence to a board shop. When I output documentation, I have folders for assembly data, bare board data, and testing data, and everything goes in each particular folder. If something's for assembly, you grab the whole folder, which has anything that may deal with the assembly world or test world or bare board. It's good to have that reminder. Another resource is your magazines. You've published information on what average documentation looks like, but I wonder how many designers look at that list and say, "What is that?" They don't even know what it is.

Shaughnessy: I know that the post-processing part is usually a designer's least favorite part of the cycle. Designers focus on the board and not documentation.

Gaines: Right. I love engineers, and I've worked with a lot of great ones, but many of them tend to be detail-oriented regarding the circuit de-

sign. But from a board layout standpoint and what is required from that point on, they were probably never taught it. They're just flying by the seat of their britches, and when somebody tells them to get it, they'll do it. I went to the Design-2-Part show a while ago in Atlanta, and I met with a company who told the guy who had done their board layout that they needed a basic netlist out of the software, but he didn't even know what he was talking about. Many don't know what they don't know.

Shaughnessy: Right, and how do we show them? What can we do about it?

Gaines: I love webinars; they're one of the best, cheapest formats for information out there. If I'm doing a board layout, I'll pop a webinar up on the screen, even if it's something I'm not interested in, just to broaden my knowledge. If I get five minutes' worth of information out of that one-hour event, that was time well spent.

Shaughnessy: Engineers and some designers still don't realize how much power they have at their station. To some extent, they can control the cost of the final product and the re-



liability, and I still think they sell themselves short in a way.

Gaines: Sometimes, designers look at board shop specifications of what they can do, not that the board needs that tight of geometry, but they can do it, so that's what they put on the circuit board. Some eight-layer boards that could easily be reduced to six-layer boards, or 14 reduced to 10. Just look at it, decide what you need, and don't think, "I'm just trying to do a board and get it off my desk."

Shaughnessy: Because everybody's rushed.

Gaines: In this world, if you're not rushed, then you're probably not needed (laughs).

Shaughnessy: What advice would you give to a new designer on how to take control and be aware that they can help make the product profitable?

Gaines: Look at a broad spectrum of standards of what's required for different designs. Technologies will drive what you're going to have to do with space and clearance, but don't put yourself in a corner. Be open to other people's opinions because one supplier on this product may ask for something while another supplier may ask for something completely different. You need to be understanding and ask questions. Make a list of what you need for the next time you're going back through it again.

I have default output files that I call up with everything; all I have to do is change a file name, click a button, and it outputs everything. I don't care if it's a board with four parts on it or one that has thousands. They all output the same pack of data. I send everybody that data, and if they choose not to use half of it, that's fine. I won't get a call back, saying, "Please send me this." Too much data is probably the right amount.

Shaughnessy: That's good. Thanks, Albert.

Gaines: Thank you, Andy. Good to see you.

DESIGN007

KLM Partners With TU Delft to Make Aviation More Sustainable



KLM President and CEO Pieter Elbers and Dean of the Faculty of Aerospace Engineering at Delft University of Technology (TU Delft) Professor Henri Werij have signed a new cooperative agreement to work together on making aviation more sustainable at the IATA Annual General Meeting in Seoul.

KLM will be contributing towards TU Delft's research into an innovative flight concept known as the "Flying-V," which embraces an entirely different approach to aircraft design, in anticipation and support of sustainable long-distance flight in the future.

Although the plane is not as long as the A350, it does have the same wingspan. This will enable the Flying-V to use existing infrastructure at airports, such as gates and runways, without difficulty and the aircraft will also fit into the same hangar as the A350. What's more, the Flying-V will carry the same number of passengers—314 in the standard configuration—and the same volume of cargo, 160m³.

The aircraft's v-shaped design will integrate the passenger cabin, the cargo hold and the fuel tanks in the wings. Its improved aerodynamic shape and reduced weight will mean it uses 20% less fuel than the Airbus A350, today's most advanced aircraft.

The Flying-V is propelled by the most fuel-efficient turbofan engines that currently exist. In its present design, it still flies on kerosene, but it can easily be adapted to make use of innovations in the propulsion system—by using electrically-boosted turbofans, for example. (Source: KLM)



Design for the Unknown

Feature by Kelly Dack, CID+

Our industry loves DFX, also known as the “Design Fors.” As PCB designers, we not only design for manufacturability (DFM) but we design for assembly, reliability, cost, test, and many more factors which we like to lump together as DFX. But now, I think it’s time we embrace a new DFX: Design for the Unknown, or DFU.

I’m a firm believer that electronics development really does start with the PCB designer. I am a big fan of Stephen Covey’s *The 7 Habits of Highly Effective People*. I especially like to practice habit No. 2 when beginning a new PCB project: Start with the end in mind. All too often, project teams seem to push ahead with only what is known about a project at the time, even to the point of starting the PCB layout. Proceeding on risk is a strategy that project teams use to make progress on a project despite not having all of the data or constraints.

But proceeding on risk may have only a small chance of working out. When incorrect assumptions are made about a product, great amounts of resources will most certainly be wasted. Years ago as a salaried PCB designer, I’d eagerly pushed ahead on design layouts overnight, on risk, only to be informed by a program manager the next morning that an assumed board outline or component needed to change. This affected the entire layout! Assumed risk in these cases obliterated hundreds of healthy sleeping hours of my life that I’ll never get back. I needed a new strategy.

Thereafter, besides committing to design PCBs on an hourly basis, I sought to discipline myself to get all of the blanks filled before starting a PCB layout. I would do better at starting a PCB layout with the end in mind because “the end” is the culmination and validation of so many critical details which the design started with in the first place.



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Where will this PCBA be manufactured? What types of equipment will be used? What are the potential volumes? What is the environment in which the PCBA will operate? How about that materials list—are we sure all of the parts are available? It all begins with design and to me, designing with the end in mind means putting all of the parts together in an organized way which would facilitate meeting all of the PCB performance and manufacturing constraints.

But in the past, I found myself waiting for the blanks to be filled in. The project timelines began to slip and I had not even begun placement of any of the parts. Slap! (Figuratively, of course.) I vowed to never again find myself in the awkward position of having nothing to show at the end of a project timeline. “I’m waiting on...” is never a good strategy. Corporate management folks who report to stockholders would rather show a poorly designed PCB progress as opposed to no PCB at all.

“The end” is filled with a myriad of details which must be considered in order to do a good job of putting the *Design* in our DFX acronym. Sometimes the design constraints at the start of a project appear fuzzy or nonexistent. Sometimes, even during the project, the goal posts change width or distance. There is rarely a perfect scenario in the world of project timelines, communication and time-to-market constraints.

One obvious question: “How can you design for something you can’t see?” You can’t, but you must. At the start of a project, unknowns will exist. You must develop the attributes of

a detective to anticipate potential fallout from the unforeseen and use practical techniques to design around them.

Times have changed. We used to hear a great deal about the benefits of products that were “designed from the inside out.” Back when automobiles were the size of large boats, we often saw ads featuring a human silhouette poised in a comfortably seated position. Roominess and comfort seemed to be the selling point of these ads. Bigger was better back then.

The Rise of the Industrial Designer

Today, smaller is better, and industrial designers typically have the first say on the overall size, shape, texture and color of a product. Products are rarely designed from the inside out now. Over time, advancements in materials and technology have offered enhanced capabilities within increasingly smaller and smaller packages.

Now, I have spent a great amount of time writing and speaking about how important it is for PCB designers to consider all of the downstream stakeholders of a PCBA project. I like to think of design as the hub of a product’s success; we must consider the needs of all of our manufacturing stakeholders downstream. If the PCB incorporates all of the DFs—design for manufacturability, design for cost, design for test, etc.—then the product is sure to be a success, right?

Well, the industrial designers of today may be akin to the fly in the designers’ proverbial oatmeal. These folks are *creatifs* whose design methodology cannot always follow the considerations of DFX. They often work directly for the inventor. Their job is to conceptualize and please the inventors, their marketers and their investors. When marketing wants the product smaller, the industrial designer can whip out a pastel marker or tap out a keystroke using some artistic software and shrink the hell out of the package envelope to the applause of the inventor while in total disregard for the unforeseen challenges they may be creating for their downstream PCB stakeholders.

“Shrinkage” was an unfortunate, unforeseen problem featured in the 85th television episode

of “Seinfeld” in 1994. But since 1994, the unforeseen challenges presented by industrial designer’s shrinking packages and its effect on IPC levels of manufacturing producibility has only made PCB design packaging and layout more perplexing. With package shrinkage, the typical product design iteration cycle goes something like this:

1. Product invention requires competitive advantage in capability, size and cost shrinkage
2. Product idea goes to industrial design to be aesthetically and ergonomically conceived
3. Product renderings go to mechanical engineers to create enclosure tooling
4. Product specifications go to Electronics engineers to locate electronic parts
5. Electronic parts are placed into schematic and BOM
6. PCB designer begins layout with PCB outline and keep-outs from ME and BOM and schematic from EE
7. Only 50% of parts will fit on PCB outline.
8. EE must shrink parts and consider two-sided assembly
9. PCB designer manages to fit parts within PCB outline though part-to-board outline spacing is compromised. Some clearance issues are mitigated by shrinking some land pattern geometry though solder joint reliability is now compromised
10. Another problem arises: limited board surface real estate on board surfaces for routing
11. PCB design must go to multilayer stackup to allow routing and power distribution

Now, the PCB cost quotation exceeds the target cost model for the project. It is only at this point, far downstream from the concept renderings phase, that the entire product must be re-evaluated for feasibility.

Rinse and repeat the entire process. Or we can try to change this process. After all, we’ll never get back this wasted time and resources.

Design For the Unknown

As PCB designers in this early, critical stage of design, we served as the project team’s reality checker. We didn’t really get to design much at all. Too many critical PCBA design attributes and constraints were unforeseen by the upstream stakeholders, rendering the concept unfeasible in this configuration. So now that the project is a prime candidate for DFU (or a redesign), how can a design team do a better job?

Project teams must embrace the concept of designing with the end in mind. From project conception on, everything will flow downstream. After all, what river raft guide would float a team of tourists down an unknown, un-navigated river?

While the design is still in the earliest stages, check in with all of the knowledgeable folks downstream—the PCB designers and all of the process stakeholders who reside downstream—and gain their design feedback. When you’re in DFU mode, you will avoid the perils of the unforeseen. Design and, if necessary, redesign with the end in mind and try leaving a little bit of extra space to make any future DFU efforts more navigable.

I hope that by working with Design007 on this idea, we can start an industry-wide discussion about DFU, and how this can help all of the stakeholders involved in developing electronic products. Feel free to drop me a line, and let’s get this conversation going! **DESIGN007**



Kelly Dack is an IPC CID instructor with EPTAC. He has over 30 years of experience in PCB design. To contact him, [click here](#).

Clear Communication Takes the Cake

Tim's Takeaways

Feature Column by Tim Haag, CONSULTANT

An amazing thing happened just a few days ago, but before I go into detail about it, let me give you a little context to better explain it. First, let me be blunt; I am not a chef. Yes, I did spend time flipping burgers professionally as a teenager, but other than that, my repertoire of culinary delights is pretty limited. A lot of this has to do with my lack of patience. Let's face it; when it is time to eat, I hate trying to figure out how to cook it.

Coincidentally, this lack of patience has made me very popular with the fast food industry. Aside from some breakfast items (including a really cool breakfast sandwich), minute rice, and [exploding chicken on the barbecue](#), I'm kind of a dunce in the kitchen. If it's peanut butter and jelly sandwiches or microwaving leftovers, I'm your guy. But for everything else, I am way out of my league.

That is why I have to honestly wonder what in the world I was thinking a couple of days

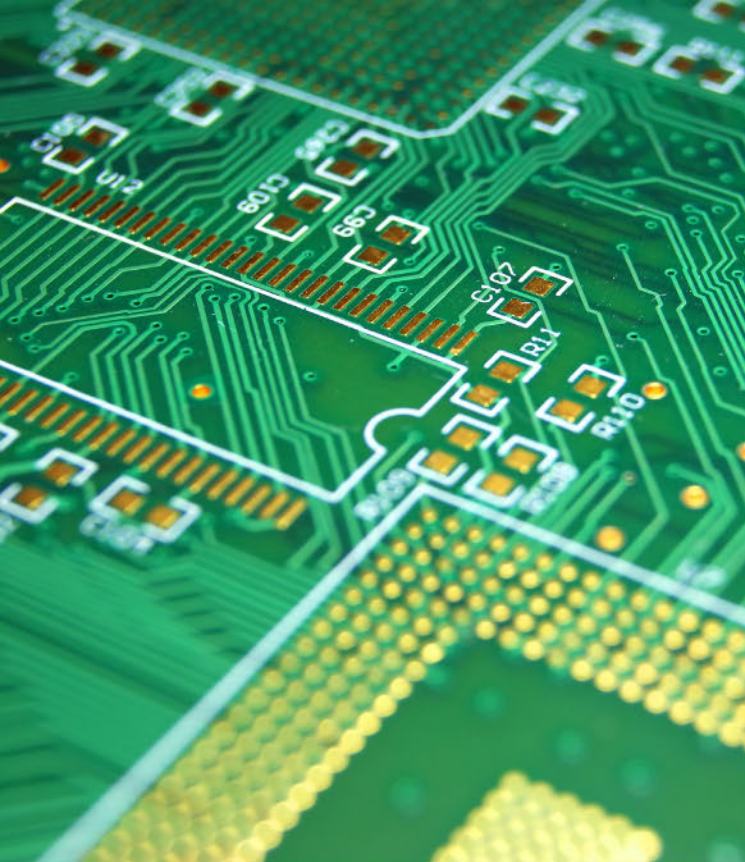
ago when I decided to make a cake for my wife on her birthday. I had already ordered a store-bought cake for the occasion (it was a chocolate-chocolate chip Bundt cake if you wanted to know), but then she mentioned that poppy seed was her most favorite cake flavor ever.

You can never have too much cake for your birthday, I reasoned, so I declared that this was going to be the year of the over-abundant birthday desserts. After a little research, though, I found out that there wasn't a bakery close enough that could provide me with a poppy seed cake, so I decided to make it myself. "What could go wrong?" I thought, forgetting for the moment about the exploding chicken on the barbecue incident, which caused the backyard neighbors to nearly call the fire department. It should also be noted that I had never baked a cake before—not even from a box mix. Realistically, my chances of success were not good.

The amazing thing that I first mentioned that was a real shocker was that the cake turned out perfectly (Figure 1). It raised like it was supposed to and tasted delicious. My wife absolutely loved it, and all of the neighbors celebrating with us were equally impressed. As much as I would love to pat myself on the back and take a bow on center stage, the truth is I owe this success to one thing and one thing only: I had



Figure 1: Perfectly baked poppy seed birthday cake.



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a great set of instructions and an easy-to-follow recipe for making this cake.

No matter if you are baking a cake or building a circuit board, it's all about clear communication. If the person writing the recipe had not made the choice to clearly communicate what their intentions were for baking that cake, I would have been lost. A missing ingredient here or an incorrect oven temperature there and my birthday surprise would have ended up in the garbage in the same way a successfully built circuit board starts with clear communication from the designer. Circuit board manufacturers want to create a perfect PCB for you, but they can only do so to the extent of the instructions that you give them. Everything truly does start with design, and whether you have success or not is up to you and how you communicate it.

To clearly communicate your "recipe" to your board manufacturers, you need to make sure that you include all of the data that they will need to get the job done correctly. This will include variations of the following data files at a minimum for both fabrication and assembly:

- **PCB image files:** These are typically Gerber formatted data files with their accompanying apertures assignments
- **NC drill files:** Excellon formatted data files that have been the standard for years
- **Fabrication drawings:** These should include board layer stackup information and drill sizes with their quantities and locations; they should also include dimensions of the board and any unique cutout features as well as detailed notes for the fabrication of the bare PCB
- **Assembly drawings:** These should include component locations and their reference designators as well as unique assembly details, such as mechanical features and any necessary mounting hardware; there should also be callouts for markings and labels as well as detailed assembly notes
- **Bill of materials (BOM) report:** This will be a data file that lists the details of each part on the circuit board

- **XY location file (pick and place):** This report details the XY location of each part on the circuit board for automated assembly equipment
- **Netlist:** This file will include all of the connectivity of the PCB for automated test routines that will be run by the manufacturer

As I said, this is just the minimal amount of data to tell your manufacturer what your PCB design needs to be built. You can do a lot more to improve communication and make your intent even clearer.

When I was baking the cake, I had a great set of instructions in the recipe I used. But the problem was that I didn't necessarily understand all of the detailed instructions in the recipe. For instance, I didn't understand what it meant to "butter and flour the cake pan," or "fold the eggs into the mixture." Hey, don't laugh; if you've never done this before, you might wonder how you "fold" eggs as well. Fortunately, I was able to find some help from online videos, and I quickly learned these little treasures of successful baking techniques.

In the same way, we too can add additional helpful instructions to our manufacturing files in the form of "README" files. These can be as simple or as complex as you want to communicate information that is above and beyond what you already have in your regular manufacturing files. The key is to make everything as clear as possible with your manufacturer. This also includes providing them with your design database if necessary. Many PCB contract manufacturers now prefer working with your entire PCB design database, especially when building prototype boards. This way, they have immediate access to schematic and netlist information that they know is synchronized with the layout information.

Another way to give your manufacturer more complete information is to use an IPC-2581 formatted output file. These files contain all of the PCB manufacturing data that the fabrication and assembly shops need to build your board. Many PCB design systems now have the capability to export manufacturing data in this for-

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mat with a push of a button. You should give this format some serious consideration if that is an option for you and your manufacturer.

Now, if you will forgive me for droning on and on about this cake that I created, there is one more comparison in this story that I would like to explore. I would not even have known that poppy seed was one of my wife's favorite cake flavors if I had not been talking to her about it first. I also wouldn't have known about some of the baking tips that I needed if I had not talked to my daughter-in-law and others about how best to do this. My point is that the most effective communication starts before you are ready to build the product so that you are ready for the task ahead.

One of the best things that you can do for yourself when getting your PCB design built by a manufacturer, is to begin talking to them before you start the design. I have heard fabrication and assembly people talk about the successes they've had working with the designer ahead of the build, and the problems they've experienced when there hasn't been adequate communication. The more communication they have with you, the better the results are likely to be.

Here's a little design treasure that I learned a while back, and hopefully it will be helpful to you too. Your manufacturers know a lot about building circuit boards because it's their job to know, and they wouldn't still be in business if

they didn't have this knowledge. They have a very good understanding of PCB materials and layer stackups and what needs to happen to configure the board for the type of design that you are doing. Ask them for help if you don't understand, and listen to their different options for performance, price, and manufacturability. With their expertise, they will be able to narrow the options down for you to give you the best value and performance for the money that you will be spending.

Remember that clear communication is the key to getting the job done right. Just as a well-written recipe helped me to be the big hero a couple of days ago on my wife's birthday, open communication and clear instructions help you to be the hero on your next PCB design. Everything starts with design, and that means that you have to take charge of making sure that everybody knows what you need to be done for the job to be successful. Now, if you will excuse me, there's only one slice of that cake left, and I want to snag it before someone else beats me to it. **DESIGN007**



Tim Haag is a PCB design consultant based in Portland, Oregon. To read past columns or contact Haag, [click here](#).

New Interaction Between Thin Film Magnets Discovered

We ubiquitously stream videos, we download audiobooks to mobile devices, and we store huge numbers of photos on our devices. In short, the storage capacity we need is growing rapidly. Researchers are working to develop new data storage options. One possibility is the racetrack memory device where the data is stored in nanowires in the form of oppositely magnetized areas, so-called domains.

A research team from Johannes Gutenberg University Mainz (JGU) in Germany, together with colleagues from Eindhoven University of Technology in the Netherlands as well as Daegu Gyeongbuk Institute of Science and Technology and Sogang University in South Korea, has made a discovery that could significantly improve these race-

track memory devices. Instead of using individual domains, in the future one could store the information in 3D spin structures, making the memories faster and more robust and providing a larger data capacity.

The Mainz-based researchers examined a number of different combinations of materials grown in multilayers. They were able to show that this previously unknown interaction exists in different systems and can be engineered by the design of the layers. This opens up the possibility of designing various new three-dimensional spin structures, which could lead to new magnetic storage units in the long term.

(Source: Johannes Gutenberg University Mainz)

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WHAT DO YOU
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Technically Appropriate Material Choices Are Key to Success

Feature Interview by Nolan Johnson

Materials are no longer a passive part of the design; they play an active role in the manufacturability, reliability, and speed of a PCB. I-Connect007's Nolan Johnson and Mike Creeden, founder of San Diego PCB Design, discuss several key characteristics that designers should consider in their material selection process.

Nolan Johnson: Mike, could you introduce yourself and tell us about what you're working on?

Mike Creeden: I'm the founder of San Diego PCB Design, and I had the opportunity to sell the company to Milwaukee Electronics/Screaming Circuits, so we've joined the Milwaukee Electronics family of companies. I also serve as an EPTAC instructor for the IPC CID and CID+ programs as an MIT (master instructor).

Johnson: We're focusing on the latest developments in materials, and it's important to get a designer's perspective. Who do you

see as being the leading companies in this segment?

Creeden: When I think of the different materials and products that are out there, one company comes to mind. So, I'm going to give some props to Insulectro, which is a distributor for many of the major laminate material products. I want to talk about them because there's a difference between good and great companies. A great company is one willing to go outside of the norm, do something that helps the designer, and supports technology development.

Their main customers are fabricators, yet time and time again, I've seen them supporting designers by trying to enhance their technical knowledge and capabilities. San Diego PCB has been collaborating with Insulectro for several years now and is looking for ways to collaborate more. They're helping us to design better, and we're utilizing products in a timely manner as they're helping us solve our customers' problems. To me, Insulectro is a significant player in this electronics material industry.

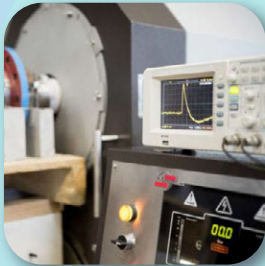


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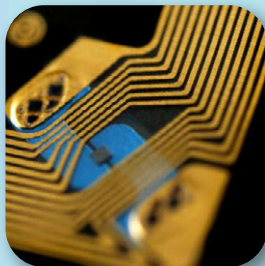
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Johnson: Could you give some examples regarding how they're helping and contributing?

Creeden: Absolutely. When I'm challenged with real estate and cannot put the required capacitors on the board because I have BGAs on both sides of a board, the team at Insulectro is a resource I can go to and ask for technology help. They suggested buried capacitance materials, which helps my power delivery and filters out noise on the board. Another example is that we're seeing a lot more rigid and rigid-flex circuits. Insulectro has coached us to utilize materials that are appropriate for these types of boards, which has helped us grow in our understanding of rigid-flex development.

Further, they point us toward their fabrication partners, which is their customer base, and this helps us understand both the material and process. There's always a learning curve for designers when it comes to rigid and rigid-flex. Some of the Pyralux materials that DuPont brings have also been useful for us trying to get our product right from the beginning. Additionally, I'm seeing more microcircuitry and some very fine features that pose a challenge. Some of the dry-film materials that DuPont offers help us with circuits that require accuracy in the definition of microfeatures.

Johnson: What's intriguing to me is that you're talking about materials early in the process. You're talking to materials experts as you're trying to figure out the layout of the board. When in the design cycle should PCB development people consider material selection?

Creeden: That's a great question. It should be within the first days of starting your project because that's the best time to establish that things will be designed "correct by construction." I do not want to design a product and then consult my fabricator in the last days of development. If the material is not in stock, we



Mike Creeden

may be delaying the procurement of what is probably a late design, anyway. You'd want to make sure that it's in stock, and you'd also want the coaching from your fabricator and supply chain to make sure that you're making correct selections. When you do this late in the process, selections may happen quickly, and there may not be enough time to ensure that it's an appropriate material selection. There's always a material technology decision,

and it should be made early in the design process. The earlier, the better because this allows time to change it if that is required.

Johnson: You're making the point that material is becoming increasingly important. With that in mind, and especially for anybody who's newer to this, why is material important?

Creeden: If you've ever seen lightning strike in the air, you're probably seeing it from the cloud to the ground. Or if you've ever seen static electricity, when the lights are low, you can see the spark fly. That's a good visualization to understand every time you're routing a trace. Historically, circuitry traces were DC in nature, and their environment didn't matter as much. Now, you are managing an electromagnetic field. The field is capacitive, and that's best (high capacitive) when a trace is close to its return path. It's also magnetic, which is inductive. That is how a signal propagates (low inductance) down the line. You're also managing an EM energy field; you're not just connecting two points with a trace. The energy field is not in the trace. Rather, the trace and its return path—typically a GND plane—serve as reference points; thus, the energy exists in the dielectric material between them. Therefore, the material with all of its parameters are an integral part of the performance of the circuit. **DESIGN007**

To read this entire article, which appeared on *Design007*, [click here](#).



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PCB007 Highlights



IPC's D.C. Focus: Chemicals Regulations, Lead-Free, Export Controls ►

From North America to Europe, Asia, and beyond, the future of the electronics manufacturing industry is shaped in many ways by government policies. That's why IPC maintains an active, multifaceted government relations program, including leadership and networking opportunities for member company executives.

The PCB Norsemen: My Flexible Story—Flex Circuit Development Through the Decades ►

Senior Technical Advisor Jan Pedersen is celebrating 26 years at Elmatica. In this column, he shares his thoughts from his long experience in this exciting industry, and talks about those things that have changed a lot in the past few decades, and the others that haven't.

DuPont on New Beginnings and Empowering the Industry ►

Andy Kannurpatti gives the I-Connect007 team an overview of the latest news from DuPont Electronics and Imaging, including investments toward the new production assets in Ohio, Silicon Valley Technology Center, and other facilities. He also details how the company is engaging OEMs and PCB fabricators and design teams, as well as some exciting business updates coming this spring and summer.

Better to Light a Candle: Chapter Two—Introduction to PCB Fabrication ►

As a reminder, "EE4800: Printed Circuit Board Fabrication" is a hands-on class intended to give engineering undergraduate students an introduction to the basics of printed cir-

cuit design, fabrication, and assembly, which started on January 14 of this year.

Trouble in Your Tank: OSP Performance—Effect of Film Thickness and Microetch ►

Two often overlooked performance attributes for organic solderability preservatives (OSPs) are the organic film thickness and the topography of the copper after microetch. Film thickness up to an extent is critical. However, the copper topography and surface preparation also play a role. Thus, you should not overlook the critical nature of the overall OSP film thickness. Read on.

New Technical Director and Upcoming 2019 EIPC Summer Conference ►

Tarja Rapala-Virtanen is the newest technical director for the EIPC. I-Connect007's Nolan Johnson and long-time EIPC conference attendee Pete Starkey discuss her new role, the upcoming summer conference in Leoben, Austria, and the program in place for the June conference.

Super PCB's Jessica Zhang on LEDs and Other Trending Business Areas ►

In an interview with I-Connect007 at the recent West Penn SMTA Expo, Super PCB Program Manager Jessica Zhang provides an overview of the company and shares new business trends they're seeing, including LEDs, wearable devices, and more.

Alun Morgan on the Future of PCB Materials ►

The I-Connect007 editorial team asked Alun Morgan, technology ambassador for Ventec International Group, to discuss materials at a high level. Our conversation delivered a detailed overview of the current state of the electronics industry.

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Modelled, Measured, Mindful: Closing the SI Loop

The Pulse

by Martyn Gaudion, POLAR INSTRUMENTS LTD.

“Which is correct—the modelled or the measured result?” A colleague posed this question to Dr. Eric Bogatin at a Polar conference many years ago. To my colleague’s evident surprise, Dr. Bogatin replied, “Neither.” Read on to find out more.

To a mechanical engineer used to laser precision in mechanical measurements, the world of high-speed electronics can seem somewhat alien. Likewise, to an electronics engineer who has inhabited a low-frequency world in a previous life and is suddenly exposed to high-speed digital, the world of ultra-high-speed serial communications can seem uncomfortably imprecise. DC voltages can be measured to many significant digits with a high degree of precision. Mechanical dimensioning in the laser age seems, and is, incredibly precise. But the world of high-speed digital signalling is less about absolute ones and zeros and more about massaging pulse shapes to squeeze them at the highest possible data rate down channels determined to squash and erode their carefully shaped waveforms.

In this woolly world where high-speed signals enter a transmission line with a well-defined shape and emerge at the receiving end eroded and distorted—and at the limits of interpretation by the receiver—it is well worth running simulation to look at the various levers that can be figuratively pulled to help the pulse arrive in a reasonable shape. At speeds up to 2 or 3 GHz, it usually suffices to ensure the trans-

mission line impedance matches the driver and receiver. And a field solver makes light work of the calculation—a little juggling with line width and dielectric substrate height will have your signals arriving in good shape. But push the frequency higher, and other factors come into play. At this point, it makes good sense to run multiple simulations and ultimately test against measurements (Figure 1).

Whilst on the subject of loss tangent, for many PCB fabricators, it is one of those “mystery” characteristics that isn’t easy to visualise or measure. The simplest way of thinking of loss tangent is to look at it as the ability (albeit undesired) to turn precious RF energy into heat. It’s excellent if you are designing microwave ovens, but not so helpful if you are attempting to transmit small amplitude high-speed signals from point A to B along a PCB transmission line. Because it is a tricky thing to

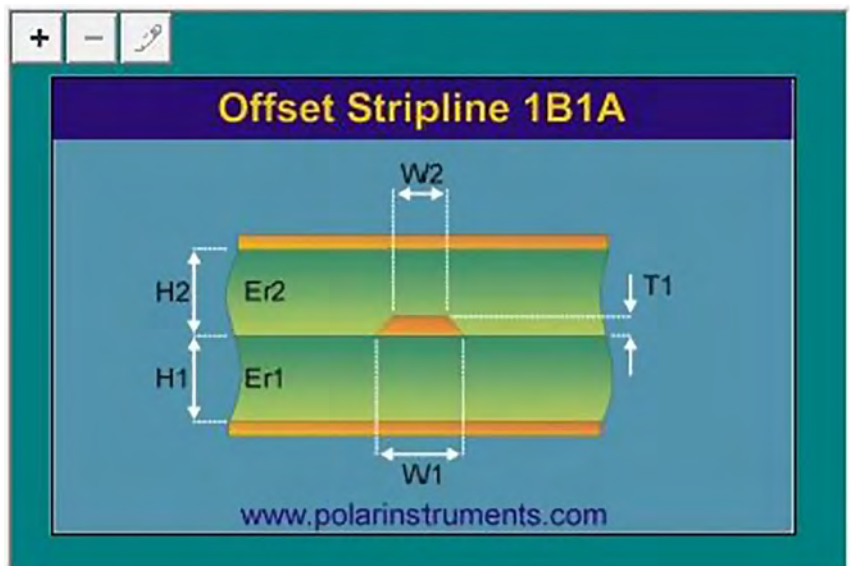


Figure 1: For lines up to 2 or 3 GHz, all you need are a few simple dimensions, a field solver, and the ϵ_r value.



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measure, it's no surprise that there are a variety of measurement methods and some more appropriate to some applications than others.

Split post resonator methods, for example, are ideal for bulk measurement of loss tangent when manufacturing base materials. When choosing a value of loss tangent for use in signal integrity applications, you will get best results if you use a value derived by using transmission line techniques. The loss tangent in a data sheet may have been measured in a variety of ways depending on application and frequency of measurement (most data sheets note this), but if in doubt, ask.

Above 3 GHz (and maybe less if the lines are long or the traces very thin and narrow), more factors come into play and modelling becomes more important and nuanced. Insertion loss

needs to be predicted, and the designer and fabricator involved in material selection or design rule selection to ensure the design operates as expected at a reasonable cost. You will need to model the effects of loss tangent on the loss as well as copper losses, which are further split into skin effect derived losses and losses owing to surface roughness. Modelling with loss tangent is relatively straightforward, and the loss is proportional to the loss tangent value and the frequency of operation. Loss tangent itself does vary with frequency, but solvers can model this for you (Figures 2 and 3).

Using the above modelling to predict Er and Tan D from a known spot frequency—in whichever is your field solver of choice and measured with an appropriate model for use in a transmission line application—is the optimum solution when faced with a variety of Tan D values, methods, and frequencies. The effects of Tan D can be seen in Figure 4 for the same geometrical structure built with low-, medium-, and high-loss materials (Tan D values of 0.01, 0.02, and 0.03).

Skin depth losses are also fairly straightforward to model. The skin depth reduces predictably with frequency. Copper roughness is a far more devious animal. The mechanical metrology is somewhat open to interpretation, and then a whole gamut of models is available, including Hammerstad, Groisse, Huray, and Cannonball Huray. They all behave in slightly different ways and obtaining input roughness data for the models is of varying complexity.

Hammerstad is the oldest method dating from WWII and the early days of radar where it was used to model the increased losses owing to machining marks on antenna waveguides. It needs Rz as input but is still a reasonable tool up to around 4 GHz. You can see in Figure 5 that Hammerstad modelling saturates both for higher roughness and frequency. Groisse is similar to Hammerstad but holds its own for a few more GHz.

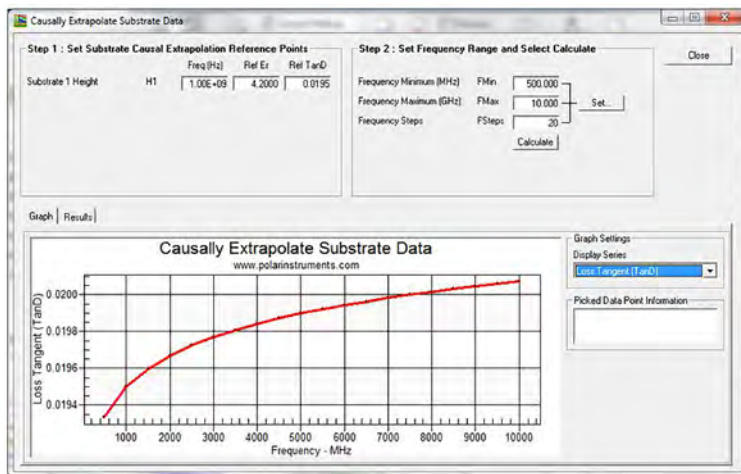


Figure 2: Tan D versus frequency.

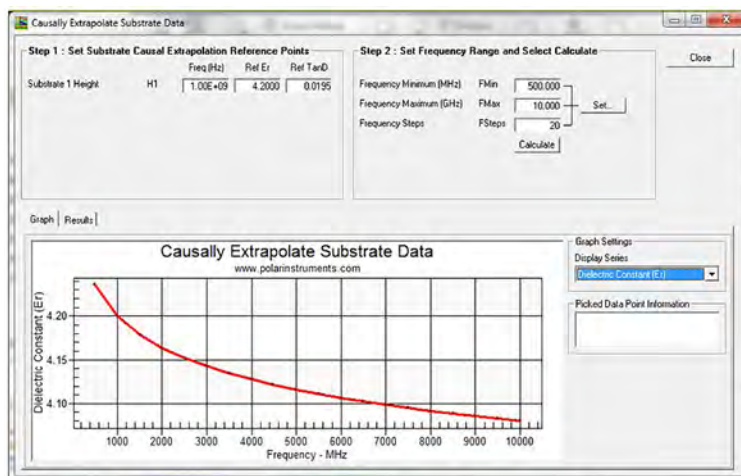


Figure 3: Er versus frequency.

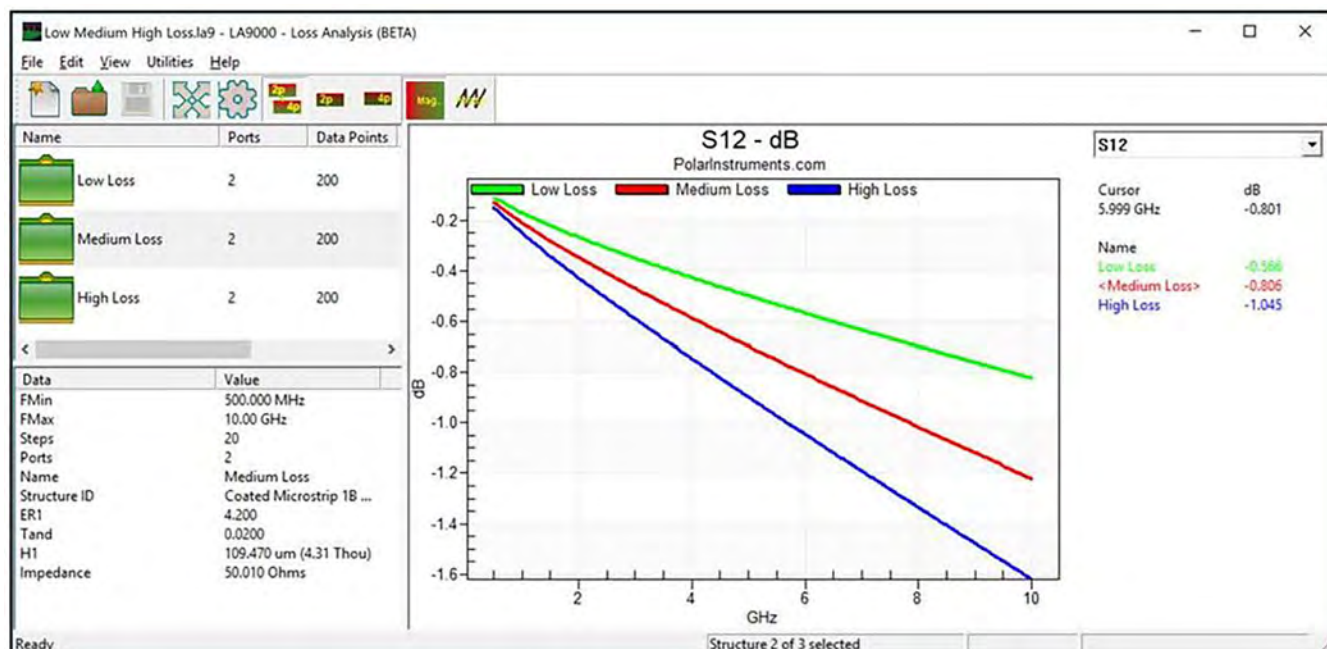


Figure 4: Low-, medium-, and high-loss materials versus frequency.

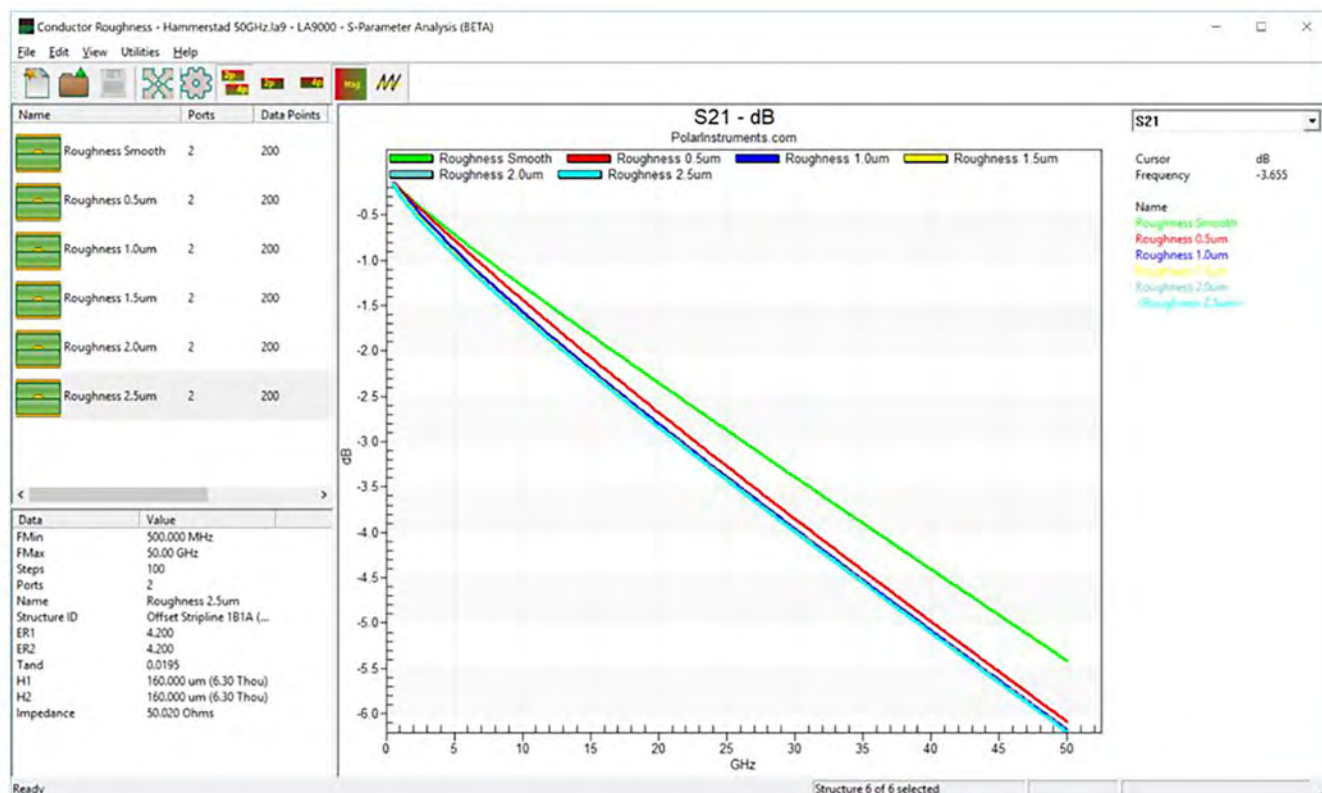


Figure 5: Hammerstad modelling of roughness losses showing saturation.

Huray is a much more recent method but requires input from a scanning electron microscope (SEM) to generate the loss figures. However, note that it does not saturate with rougher

surfaces, which is useful, as some laminates with high performance still have rough copper to promote adhesion. This is changing with newer materials, and chemical processes

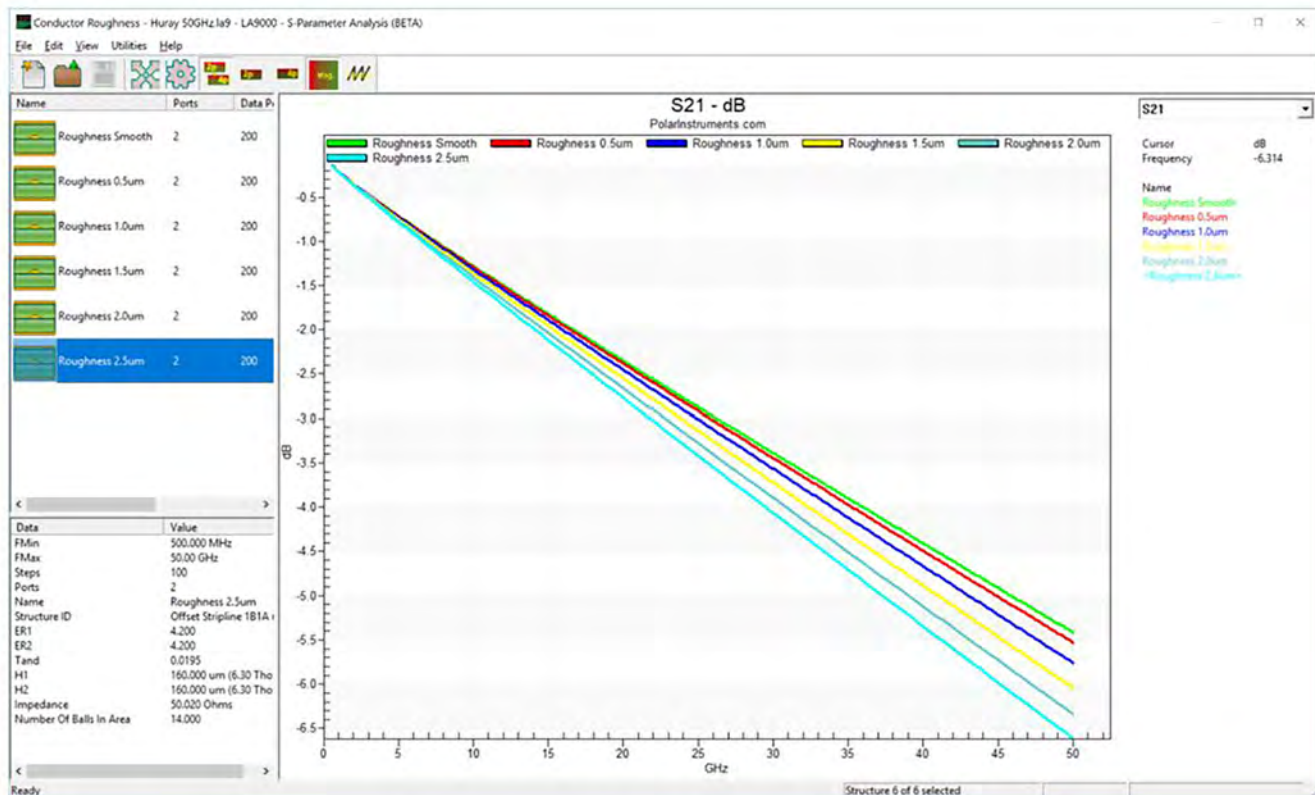


Figure 6: Huray modelling of roughness losses showing saturation.

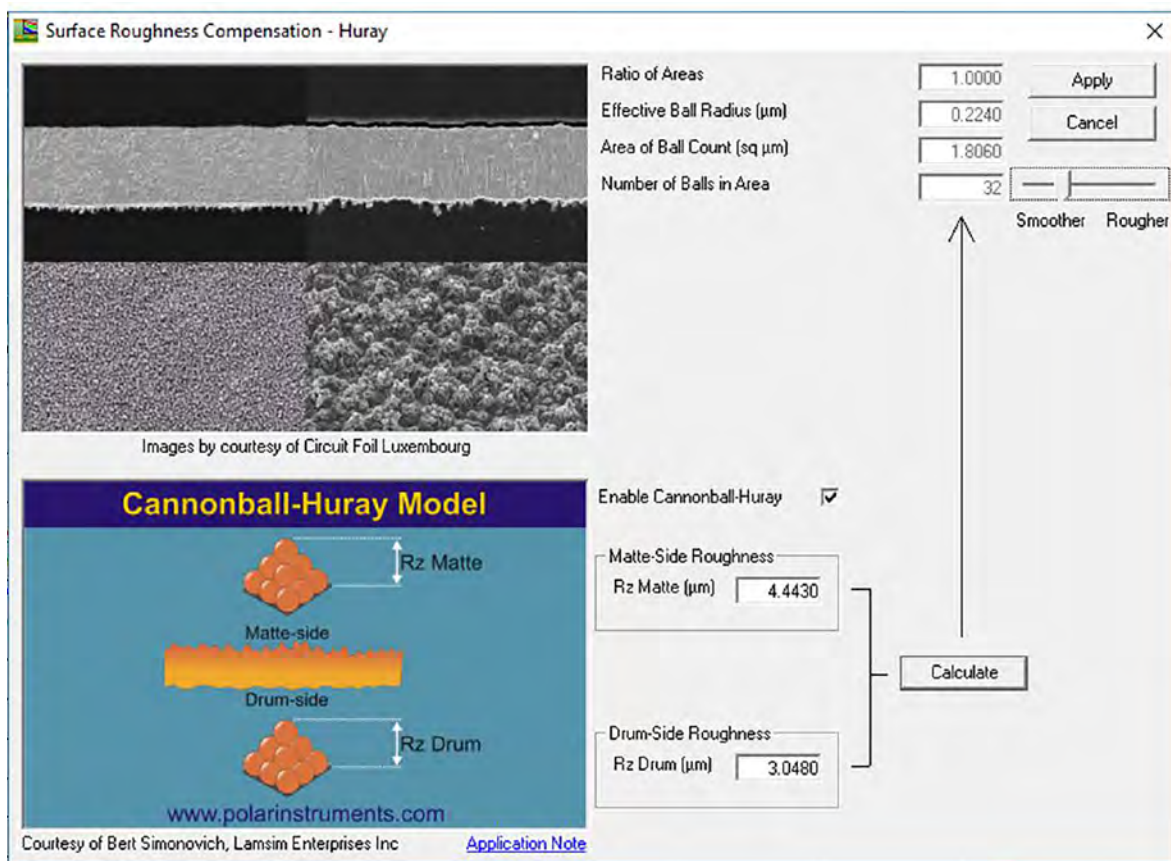


Figure 7: Cannonball-Huray model.

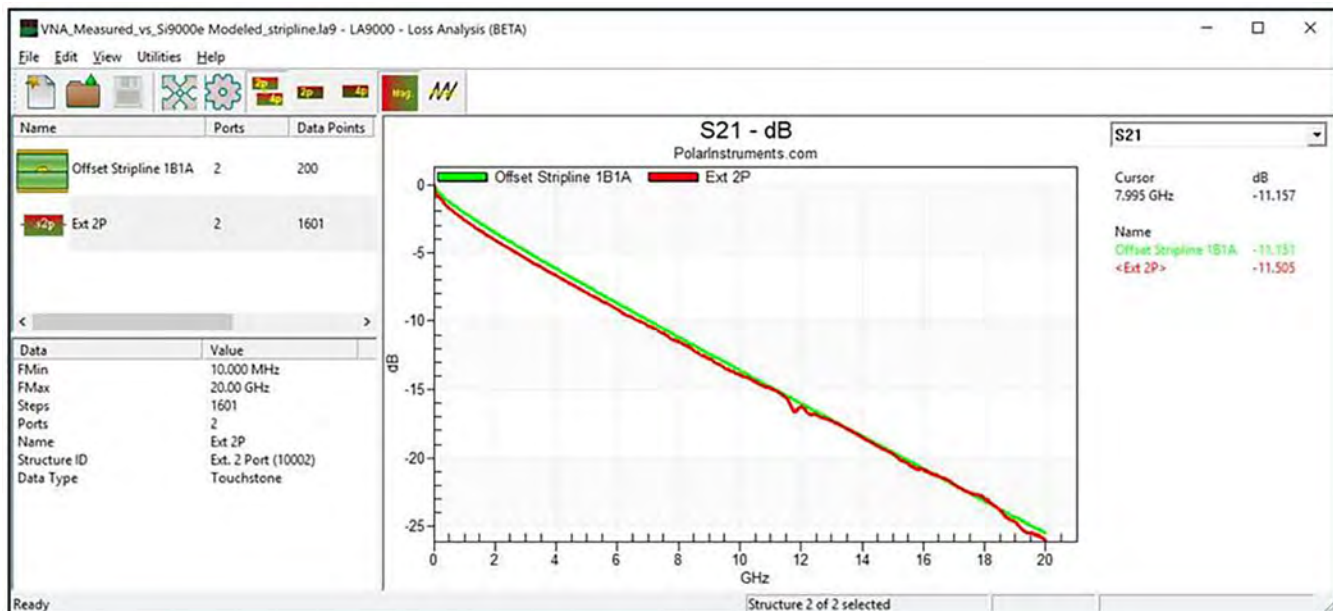


Figure 8: Modelled and measured data overlaid.

to promote chemical rather than mechanical adhesion are becoming available though at a premium (Figure 6).

Whilst Huray for “purists” requires images processed from SEM images of the copper foil, there is a very useful empirical short cut to entering viable Huray parameters from simple Rz figures. This is the Cannonball Huray input developed by Bert Simonovich at Lamsim Enterprises (Figure 7).

Once you have completed modelling, it is always good to close the loop by comparing measured with modelled. For clarity, Figure 8 shows one model versus the measured, but you can imagine overlaying a measurement result over a group of five roughness simulations to see which is the best fit as previously shown.

Conclusion

In summary, you may recall the question my colleague asked Dr. Bogatin, “Which is correct?” and his answer, “Neither.” You should look at both and at the correlation, and then use your mind to test the validity of either. Ask yourself, “Does the measurement result look credible at the frequency of interest or has it become unstable as the signal power drops into the noise floor? Does the phase align at the frequency of interest?” And regarding the

modelling, ask yourself if you have accounted for the roughness in an appropriate way. Have you rounded off the loss tangent figure and lost precision? Have you studied a microsection of the trace under test? Being aware of these items and applying mindful common sense will give you confidence in aligning modelling and measurement in a mindful way.

Glossary

Dielectric constant: The ability of how well a substrate can store electrical charge, often referred to with a variety of symbols such as ϵ_r , E_r , D_k , or K .

Loss tangent: The (undesirable) ability of a substrate to turn useful signal energy into heat (unless you are making a microwave oven.) Loss tangent is also referred to with a variety of terms, including $\tan \delta$, $\tan D$, or D_f . From an SI perspective, the lower, the better, but you need to factor in the cost. **DESIGN007**



Martyn Gaudion is managing director of Polar Instruments Ltd. To read past columns or contact Gaudion, [click here](#).

Chapter Check-ins: Orange County, San Diego, and Phoenix

The Digital Layout

by Stephen V. Chavez, MIT, CID/CID+, IPC DESIGNERS COUNCIL

In this month's column, I'm highlighting three individual IPC Designers Council Chapters at the same time, including the Orange County, the San Diego, and the Greater Phoenix Area Chapters. The three chapter presidents—Scott McCurdy, Luke Hausherr, and Randy Kumagai—share the success of recent events and activities.

Orange County Chapter by Scott McCurdy

We had our last “lunch ‘n learn” meeting April 25 in Irvine, California, with 39 designers and PCB professionals in attendance. Our speaker was Natasha Baker, founder and



CEO of SnapEDA, who gave a talk on “Mistakes Even the Best Engineers Make: How and Why to Build Better Libraries.”

Baker discussed the common pitfalls to avoid when creating libraries and shared examples of mistakes that inevitably creep into such a detail-oriented process and ways to avoid them. She has an electrical engineering background and was a knowledgeable and engaging speaker. Lots of questions came up from the audience, which provided a great learning dialogue for all who attended.

Mentor, a Siemens Business, hosted the lunch, and we appreciated their support in helping defray the cost of our chapter event. We wrapped up our meeting with raffle prizes provided by SnapEDA, Altium, Mentor, and Freedom CAD Services Inc. We look forward to our next meeting sometime in July. If you have





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any questions, you can email me at scott.mc-curdy@freedomcad.com.

San Diego Chapter by Luke Hausherr, CID+

We held our annual meeting at the Del Mar Electronics show on May 1. It was well attended, and the presentation from Gerry Partida, director of engineering at Summit Interconnect, was very well received. He shared his expertise on how fabricators process initial Gerber data, and the audience was engaged with questions and input throughout the presentation. We ended the presentation with our usual raffle giveaway with over \$11,200 in software and other prizes.

Our chapter is planning our next event in July, and we're considering meeting with SMTA and iMAPS for a dinner social somewhere fun in San Diego. Later this fall, we plan on hosting an event with a special guest speaker to talk about conformal coating applications for PCBs. We are still eagerly pursuing new membership for our chapter, so if anyone in San Diego or the nearby areas wants to join our chapter for free and participate in networking events and educational seminars, please email us at IPCDC.SD@gmail.com.



Greater Phoenix Area Chapter by Randy Kumagai

As the new chapter president, we had our first Leadership meeting to establish some goals and opportunities. We started a LinkedIn page for our chapter and received an updated list from the corporate chapter of active companies in Arizona. We will soon be hosting a chapter meeting and are investigating site locations and sponsors. If you would like to sponsor a local



chapter meeting, please contact me at rkumagai@silvermountaindesign.com.

IPC DC Executive Board

The IPC DC Executive Board and the IPC Education Foundation continue to work toward common goals. Stay tuned for more updates as we continue to collaborate for the betterment of our industry.

A Special Note From IPC and EPTAC Corporation

We have a new Master Instructor Trainer (MIT) for IPC PCB design certification CID/CID+. Stephen Chavez has been IPC approved and promoted to the status of MIT. Stephen's many years of experience, education, and continued professional development are key to his career success. He is a welcome addition to the MIT team for IPC and EPTAC Corporation. Congratulations, Stephen!

2019 Training and Certification Schedule

IPC Certified Interconnect Designer (CID)

- June 18–21: Kirkland, WA
- August 6–9: Baltimore, MD
- August 26–29: Markham, ON
- September 6–9: Santa Clara, CA
- September 19–22: Schaumburg, IL
- October 21–24: Anaheim, CA
- November 2–5: Raleigh, NC
- November 5–8: Dallas, TX

IPC Advanced Certified Interconnect Designer CID+

- July 15–18: Warren, MI
- September 6–9: Santa Clara, CA
- September 10–13: Kirkland, WA
- September 17–20: Schaumburg, IL
- October 21–24: Anaheim, CA
- November 2–5: Raleigh, NC
- December 3–6: Manchester, NH

Note: Dates and locations are subject to change. Contact [EPTAC Corporation](#) to check current dates and availability. A minimum enrollment of seven students is required for a class to be held.

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The IPC Designers Council is an international network of designers. Its mission is to promote printed circuit board design as a profession and to encourage, facilitate, and promote the exchange of information and integration of new design concepts through communications, seminars, workshops, and professional certification through a network of local chapters. **DESIGN007**



Stephen Chavez is a member of the IPC Designers Council Executive Board and chairman of the communications subcommittee. To read past columns or contact Chavez, [click here](#).

Accurate Probing of Magnetism With Light

In magnetic materials, a wealth of information can be retrieved by optical spectroscopy where the energy of the individual light particles—photons—promotes inner shell electrons to higher energies. This is because such an approach allows to obtain the magnetic properties separately for the different types of atoms in the magnetic material and enables scientists to understand the role and interplay of the different constituents.

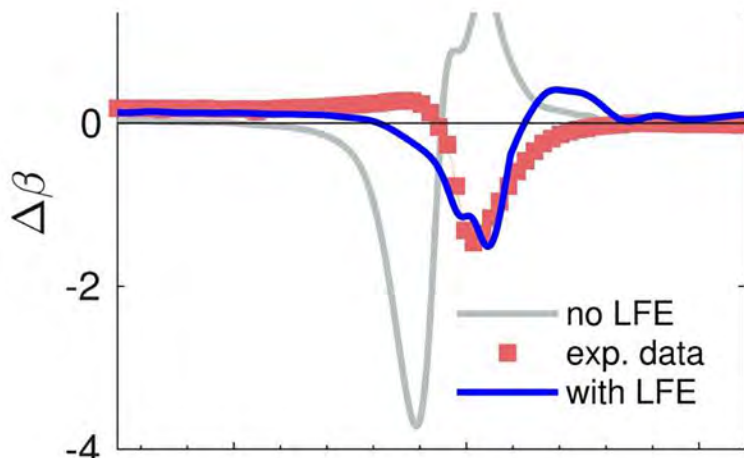
A team of researchers from the Max Born Institute in Berlin together with researchers from the Max-Planck-

Institute for Microstructure Physics in Halle and Uppsala University in Sweden has now provided a detailed analysis of the magneto-optical response for XUV photons. They combined experiments with ab initio calculations, which take only the types of atoms and their arrangement in the material as input information. For the prototypical magnetic elements iron, cobalt and nickel, they were able to measure the response of these materials to XUV radiation in detail.

The scientists find that the observed signals are not simply proportional to the magnetic moment at the respective element, and that this deviation is reproduced in theory when so-called local field effects are taken into account.

This new insight now allows to quantitatively disentangle signals from different elements in one material. “As most functional magnetic materials are made up from several elements, this understanding is crucial to study such materials, especially when we are interested in the more complex dynamic response when manipulating them with laser pulses,” emphasizes Felix Willems, the first author of the study.

[Source: Forschungsverbund Berlin e. V.]



The Future of PCB Manufacturing Doesn't Belong to Robots, but to the Users

Connect the Dots

by Bob Tise, SUNSTONE CIRCUITS

Is the world ready for the consequences of rapid automation? Will the use of robots displace entire categories of workers? Can artificial intelligence really “think”? How will manufacturing, including PCB manufacturing, be affected by all of these smart robots?

These may sound like thoroughly 21st-century questions, but they actually come from a pamphlet published in 1955. In *The Age of Automation: Its Effects on Human Welfare* ^[1], intrepid industrial reporter Warner Bloomberg Jr. wrote about the emergence of robotics in a post-war economy. The parallels to today are striking.

First, there's the media frenzy. Bloomberg alludes to the “hundreds of articles” that either warn that robotics will “lead to massive unemployment” or proclaim that the technology “will usher in a new ‘golden age’ of plenty.”

There's also the disconnect between CEOs and their frontline factory employees. “See how easy it is to make gasoline?” an oil executive remarks about his refinery's new-fangled automatic control system. “You just put the crude oil in at one end, and the gasoline comes out the other!” His ill-conceived “joke” manages to not only disparage his workforce but betray his poor understanding of the technology.

Further, there are the “smart” machines that obfuscate their critical human elements. Bloomberg mentions a state-of-the-art computer that can translate several sentences of Russian into English “in a few seconds”—that is, “after months of time put in by human experts ‘programming’ the operation.” Next, there are alarms of imminent, unimaginably vast catastrophe. One automation doomsayer Bloomberg quoted believed “the unemployment it causes

will be, given our present frame of economic thought, very large, permanent, and absolutely unprecedented.”

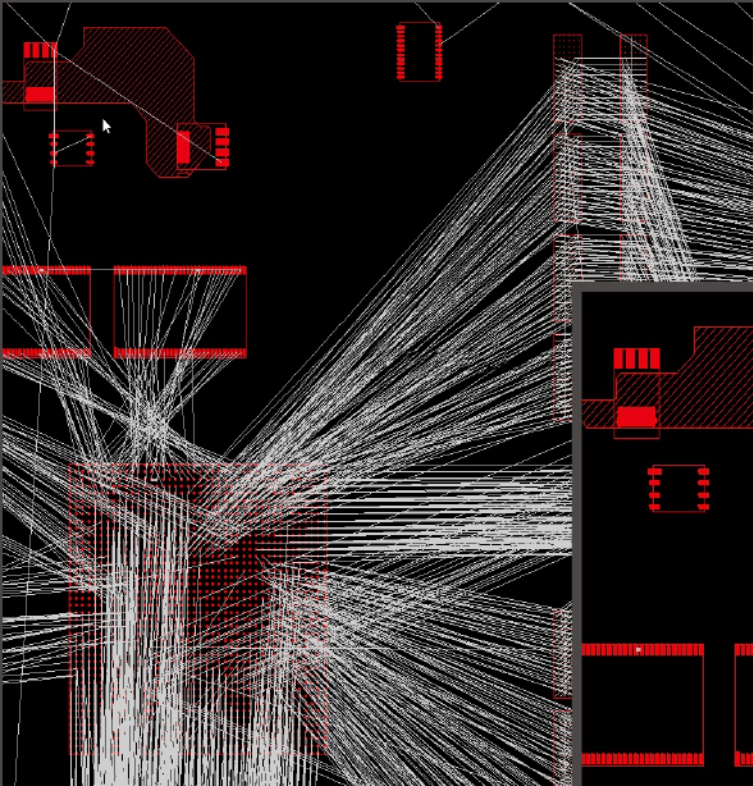
This was all in the '50s. While robotics and other forms of automation have undergone significant evolution since then—within and beyond circuit board manufacturing—our general attitudes have not.

A Robot Is a Robot Is a Robot

What do hazardous materials inspection, automotive welding, and bowling alley pinsetting all have in common? All are monot-

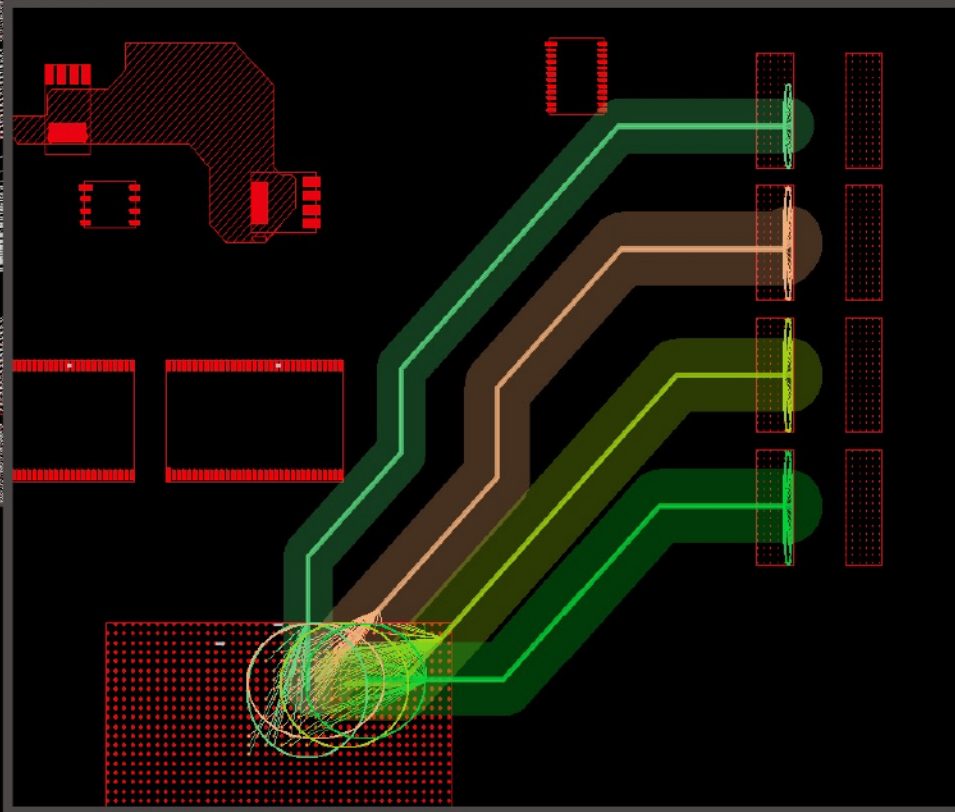


Figure 1: Smart robots are no longer relegated to the future.



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onous, dangerous jobs—and ideal for automation.

In the debate over worker displacement, people seldom mention how automation has improved worker well-being. Robots perform numerous jobs that otherwise pose health and safety risks, whether it's a major risk, such as toxic fumes, or a minor one, such as repetitive muscle strain ^[2]. In these and virtually all practical applications of robotics, a human being is still monitoring, controlling, or programming the machine.

In addition to minimizing injuries and deaths, robots excel at routine tasks that require a high degree of accuracy, repeatability, and consistency. In PCB manufacturing, such tasks include the assembly of service mount components as well as picking and placing. From chip shooters to gantry-style machines, our industry has been using robots for decades.

From chip shooters to gantry-style machines, our industry has been using robots for decades.

Can You Teach an Old Robot New Tricks?

No matter how fast or advanced a facility's robotics, humans need to direct, troubleshoot, and keep track of the work. Moreover, outside of high-volume production runs, PCB manufacturing is not an assembly line. It's hard to imagine how an automated system could be useful in low-quantity prototyping or any other non-linear, one-off process that demands multiple judgment calls.

That includes even seemingly simple processes. Say you needed three sheets of five-mil laminate with two-ounce copper thickness. Now, consider how many steps are involved in identifying, fetching, and stacking the materials. You could feed instructions into a robot, hit "go," and the robot will do the job ac-

curately, but will you save any time? Probably not. Nor are you likely to save time in the long run.

At Sunstone, each order is unique. With robots, we would need to program every step in the manufacturing process for every order. It's much faster and easier to fabricate by hand. On top of that, unlike the computers we buy, humans don't become obsolete—or at least our obsolescence takes longer. Employees can learn and be retrained. Machines need to be updated or replaced.

Artificial Intelligence vs. Artifice

"But wait," you might be thinking. "Aren't machines already taking over complex human jobs? What about artificial intelligence?" If you think AI is close to approaching anything resembling human cognition, here's some bad (or possibly good) news: What we call "AI" is hardly ever intelligent.

According to an article by James Vincent titled "The State of AI in 2019," true artificial intelligence is a long way away, and genuine breakthroughs tend to get buried under marketing "hype and bluster" ^[3]. The article names Oral-B's Genius X toothbrush, which debuted at this year's Consumer Electronics Show (CES), as one example of the phenomenon. The device's "supposed 'AI' abilities" are really based on "clever sensors" that provide "simple feedback about whether you're brushing your teeth for the right amount of time and in the right places." Dentists can rest easy, for now.

How "Futuristic" Will the Future Be?

Make no mistake—plenty of exciting developments are happening in the world of robotics; they just aren't the kinds that will lead to a Terminator-esque dystopia.

Boston Dynamics, for instance, has built machines such as BigDog and Atlas that display impressive, almost lifelike abilities to maneuver around simulated battlefield environments. Boston Dynamics' creations are not autonomous, however—a Wired interview with the team reveals movement is "mostly done by humans and remote control" and the machines "follow a well-defined set of rou-

5G: Higher Frequencies!

Do you have the **right** circuit materials?

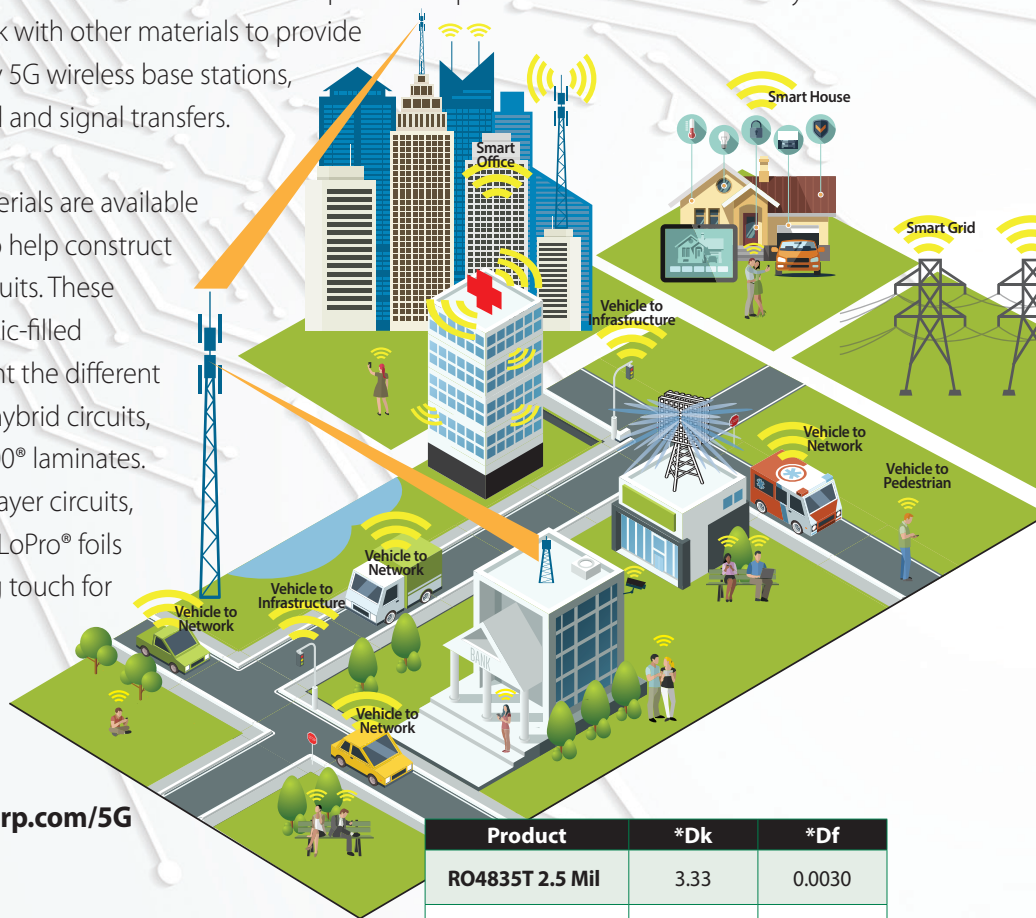
Frequencies at 28 GHz and higher will soon be used in Fifth Generation (5G) wireless communications networks. 5G infrastructure will depend on low-loss circuit materials engineered for high frequencies, materials such as RO4835T™ laminates and RO4450T™ bonding materials from Rogers Corporation!

Rogers RO4835T spread-glass-reinforced, ceramic-filled laminates are low-loss materials in 2.5, 3.0, and 4.0 mil thicknesses. They are well suited for millimeter-wave frequencies as part of the inner cores of 5G hybrid multilayer PCBs. They can work with other materials to provide the many functions needed by 5G wireless base stations, including power, signal control and signal transfers.

Rogers RO4450T bonding materials are available in 3, 4, and 5 mil thicknesses to help construct those 5G hybrid multilayer circuits. These spread-glass-reinforced, ceramic-filled bonding materials complement the different materials that will form these hybrid circuits, including RO4835T and RO4000® laminates. And for many 5G hybrid multilayer circuits, Rogers CU4000™ and CU4000 LoPro® foils will provide a suitable finishing touch for many hybrid multilayer circuit foil lamination designs.

5G is coming! Do you have the right circuit materials?

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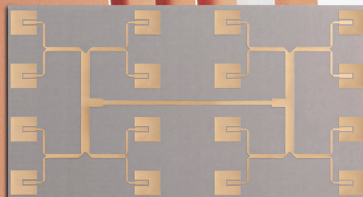
Product	*Dk	*Df
RO4835T 2.5 Mil	3.33	0.0030
RO4835T 3.0 Mil	3.33	0.0034
RO4835T 4.0 Mil	3.32	0.0036
RO4450T 3.0 Mil	3.23	0.0039
RO4450T 4.0 Mil	3.35	0.0040
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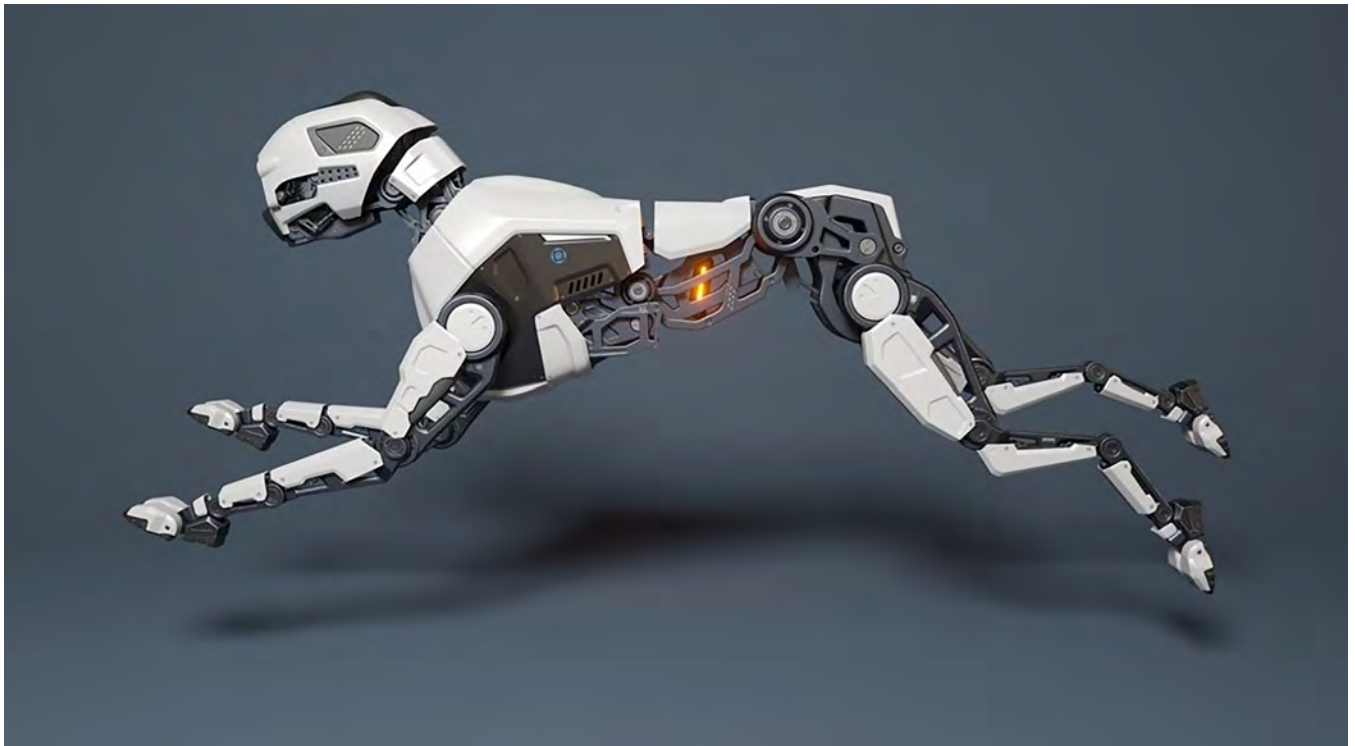


Figure 2: Lifelike robot animals like this are a reality now.

times; they don't have the ability to decide on their own what to do" ^[4]. Killer robots these are not.

Fully autonomous vehicles (i.e., self-driving cars) seemed like a foregone conclusion just a few years ago, but appear similarly out of reach now. Road tests—like the tragically fatal one Uber conducted in Arizona—have uncovered significant technical limitations and raised a host of ethical and infrastructure-related concerns.

For truly awe-inspiring innovation, look at recent developments in medical neuroprosthetics. A team of researchers at the University of Chicago is currently working on robotic limbs patients can control via electrodes implanted in the brain ^[5]. That's intelligence in more ways than one.

In our industry, robotics stand to improve numerous processes. There's water jet cutting and laser etching, for example. Or imagine a through-hole plating conveyor system that lifts and loads boards into chemical vats, rinse agents, and keeps track of dips for multiple batches in multiple stages. Or how about a robot that could produce a prototype on demand

at the click of a button? Oh, right—that's a 3D printer. Remember when those seemed revolutionary? **DESIGN007**

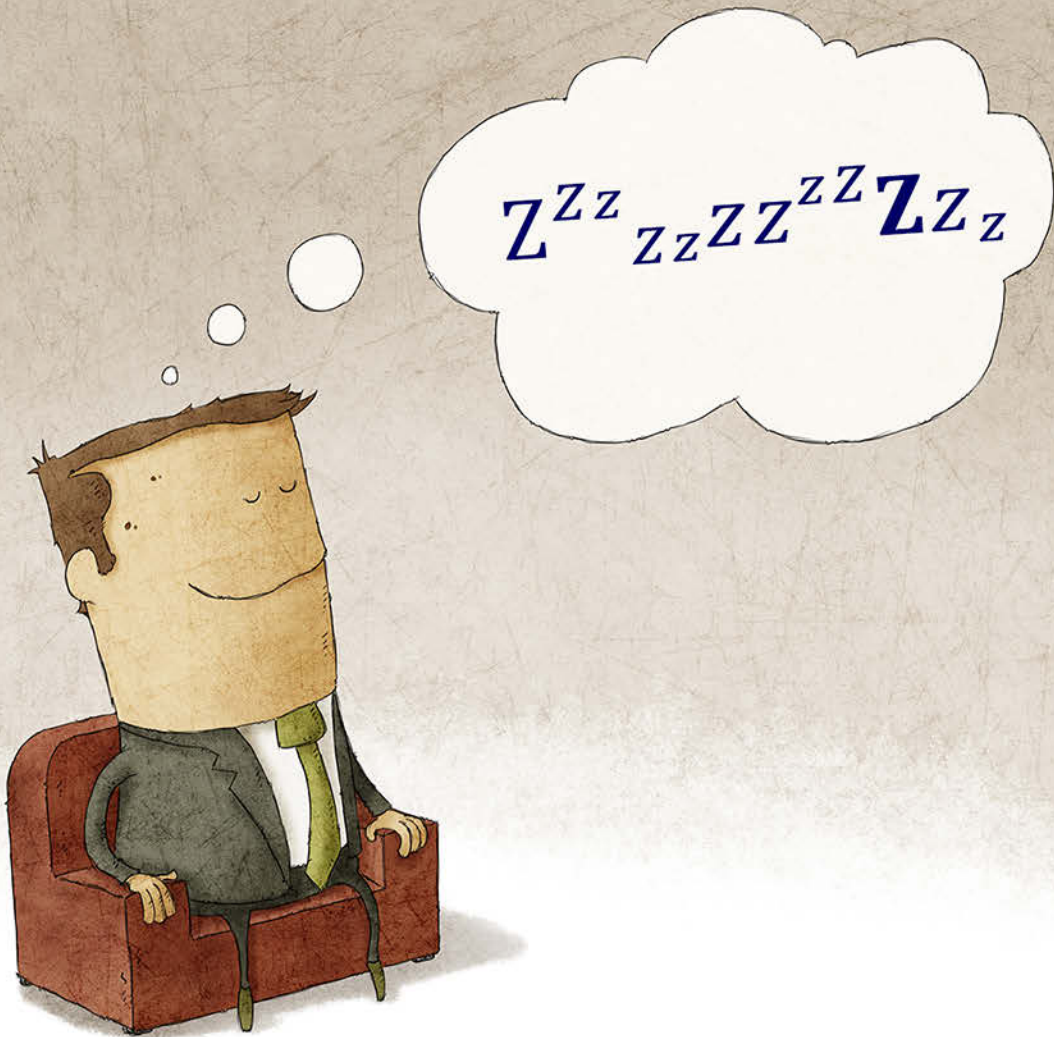
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2. Marshall, D. "[Manufacturers Employ Robots to Improve Worker Health and Safety Comments](#)," ABB Conversations, November 16, 2012.
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Bob Tise is an engineer at Sunstone Circuits. To read past columns or contact, [click here](#).

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Resins Fit for a Purpose: Failure Mitigation and Environmental Concerns

Sensible Design

by Alistair Little, ELECTROLUBE

So far, in my columns on resin chemistries and encapsulation/potting techniques, I have tended to concentrate on the properties of these materials. My insights have included how they are best applied in the factory, and the steps that must be taken to get the best performance from them once they are in the field to protect an electronic assembly or lighting fixture against the elements. In this column, I am going to address the question of resin failures—in particular, how to avoid them—and to get a better idea of where and how appropriately selected and applied modern resins are making a big difference in the world of extreme electronics installation and implementation.

Regarding resin failures and how to avoid them, there are some excellent, well-formulated

resins out there that will deliver unfailing service as long as they are carefully selected for the anticipated conditions, stored appropriately, and applied and cured according to the manufacturer's recommendations. One lapse in this sequence and you are likely to have a problem on your hands that may manifest itself on the test bench if you are lucky. But if you are very unlucky, it will manifest sometime later when a unit is already in service and likely to be operating in some hazardous or otherwise difficult-to-access location.

There are a number of simple steps that you can follow to reduce incidences of resin failure, and, at best, help you avoid them altogether. First, always read the product manufacturer's technical data sheet; this will at least guide you





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on basic requirements, such as ensuring that the correct storage conditions for the product are being maintained. Operate good stock rotation so that the resin is not left in storage for a prolonged length of time, and always make sure that containers are kept well sealed.

Second, it is vital to ensure that the correct mix ratio for two-component resins is achieved. For medium- to large-production volumes, the use of a mixing machine is recommended to minimise the risk of variability in the mix ratio across a production run. It is important that all pipework used with these machines is bled properly so there isn't any air present in the system, which could result in mix ratio variations or air entrapment in the resin.

It is always wise to carry out regular checks on the amount of each component being dispensed if a machine is used. And if manual mixing is preferred, such as for short runs and/or prototyping, it is advisable to use calibrated balances to measure each component. Only pour the amount of resin required for the job in hand and be sure to reseal containers without delay.

Cleanliness is vital to achieving satisfactory potting or encapsulation.

Cleanliness is vital to achieving satisfactory potting or encapsulation. Metal enclosures, for example, must be thoroughly cleaned before resin application to remove any corrosion, dirt, grease, or metalworking fluids that might be present as these will reduce the resin's ability to adhere to the metal surface. Similar precautions need to be taken with plastic-moulded housings to remove any residual mould release agents. Make sure that the PCB itself is clean because any dust or other contamination on the surface will get trapped. The resin will adhere to the contamination rather than to the surface of the board or components, resulting in a weak spot and a potential point of failure.

The useable life, gel, and curing times of a resin are all based on it being cured at room temperature. It is possible to reduce these times by the application of heat, but it is best to do this after the material has gelled to ensure a consistent cure. The amount and type of resin in a unit will determine the potential exotherm, which is the rise in temperature of the resin resulting from the chemical reaction between its two components on mixing. The larger the volume of resin used, the larger the exotherm. Where larger volumes need to be encapsulated, it is best to conduct this in two or more stages to minimise any potentially damaging exotherm. Check the technical data sheet for any curing recommendations for elevated temperatures but remember that every oven/curing chamber is different, so the same resin in the same volume may require a different curing profile in two different ovens.

Environmental Considerations

Resins can protect an electronic assembly against a wide variety of environmental influences, whether they are due to climatic conditions or potential attack from any chemicals to which the assembly may be exposed. One of the biggest concerns is to keep water out of the assembly from light moisture due to high ambient humidity or full immersion in saltwater.

Electronic assemblies are now being deployed and operated in environments that would not have been contemplated only a decade or so ago, and each year, more extreme environments are being specified by designers. For example, there are resins suitable for use in aquatic environments, both fresh and saltwater, from a light splash to full immersion. And resins can now be found protecting a variety of submerged applications from swimming pool lights to sensors used for monitoring pollution in rivers to telecommunication cable joints deep beneath the ocean surface.

Resin formulations are also likely to be influenced by geographical location. Polyurethane resins, for example, are particularly sensitive to moisture and have to be modified for areas with high humidity and/or rainfall. Conversely, silicone resins will require a certain amount

of humidity to enable the resin to cure. High ambient temperatures can reduce the shelf life of certain resins, and where the resin has a high percentage of fillers, these conditions can also cause filler sedimentation.

Low temperatures bring their own set of problems. When the temperature drops below 10°C for a long period, certain resins and hardeners begin to crystallise, and the crystals drop out of solution. Many materials can be heated so that the crystals are dissolved back into solution, but some cannot be treated in this way. Again, it is important to consult the material's technical data sheet to ascertain the resin's optimum storage conditions.

Always consider what rules and regulations are valid in various regions of the world and the preferences of the different industries that are to be served in these regions. The choice of resin chemistry is very likely to vary, such as for health and safety or other environmental

regulatory requirements. In some areas, epoxies will be preferred over polyurethanes, while in others, silicone resins would simply be a non-starter.

Resins play an integral part in ensuring that an electronics product can survive for at least its design life and often well beyond. Be it chemical, environmental, physical, or thermal, whatever the conditions, there is a resin system that can be found or developed to provide the protection required. **DESIGN007**



Alistair Little is global business/technical director—resins—at Electrolube. To read past columns from Electrolube, [click here](#). Also, visit I-007eBooks.com to download your free copy of Electrolube's book, *The Printed Circuit*

Assembler's Guide to... Conformal Coatings for Harsh Environments, as well as other free, educational titles.

Flexible Generators Turn Movement Into Energy

Wearable devices that harvest energy from movement are not a new idea, but a material created at Rice University may make them more practical.

The Rice lab of chemist James Tour has adapted laser-induced graphene (LIG) into small, metal-free devices that generate electricity. Like rubbing a balloon on hair, putting LIG composites in contact with other surfaces produces static electricity that can be used to power devices.



In experiments, the researchers connected a folded strip of LIG to a string of light-emitting diodes and found that tapping the strip produced enough energy to make them flash. A larger piece of LIG embedded within a flip-flop let a wearer generate energy with every step, as the graphene composite's repeated contact with skin produced a current to charge a small capacitor.

The lab turned polyimide, cork and other materials into LIG electrodes to see how well they produced energy and stood up to wear and tear. They got the best results from materials on the opposite ends of the triboelectric series, which quantifies their ability to generate static charge by contact electrification.

In the folding configuration, LIG from the tribo-negative polyimide was sprayed with a protective coating of polyurethane, which also served as a tribo-positive material. When the electrodes were brought together, electrons transferred to the polyimide from the polyurethane.

The best configuration, with electrodes of the polyimide-LIG composite and aluminum, produced voltages above 3.5 kilovolts with a peak power of more than 8 milliwatts.

(Source: Rice University)

The **Key** to Product Reliability

Beyond Design

by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

With today's rapid product development cycles and time-to-market pressures, PCB designers are pushed to their limit. This situation leaves many developers with the question of how to ensure that their high-speed digital design performs to expectations, is stable given all possible diverse environments, and is reliable over the products projected life cycle. As developers avoid the expense and delays of re-engineering the product, they look to employ design integrity methodologies during the design phase.

For a sufficiently large number of electronics products, failures are distributed in time as shown in Figure 1. This curve is called “the bathtub curve” and displays the typical reliability of diverse products regardless of their functionality. One would expect a product to fail after some years of service but preferably long after the product becomes obsolete. Premature failures are of particular concern and are typically the result of poor design practice or substandard manufacture. This column will focus on the design aspects.

The cost of development is dramatically reduced if the simulation is employed early in the design cycle (Figure 2). If changes are made late in the design process, then it takes more time, people, materials, and money to

complete the project. The advantage of simulation is that it identifies issues early in the design process and rectifies them before they become a major problem.

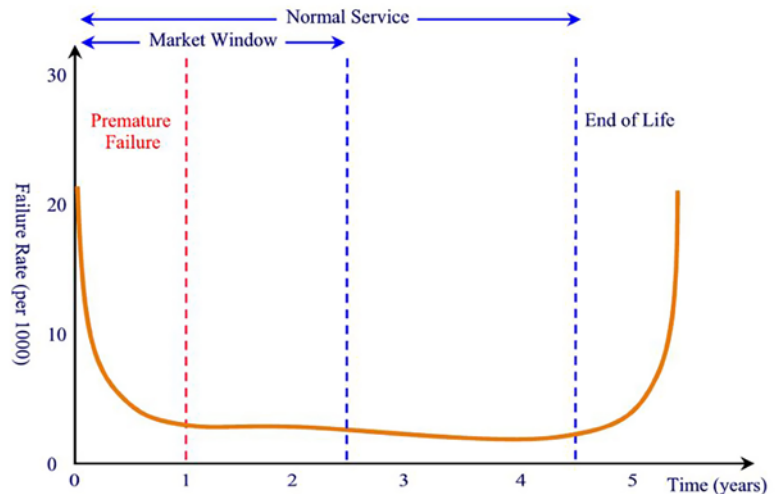


Figure 1: The bathtub curve-product reliability life cycle.

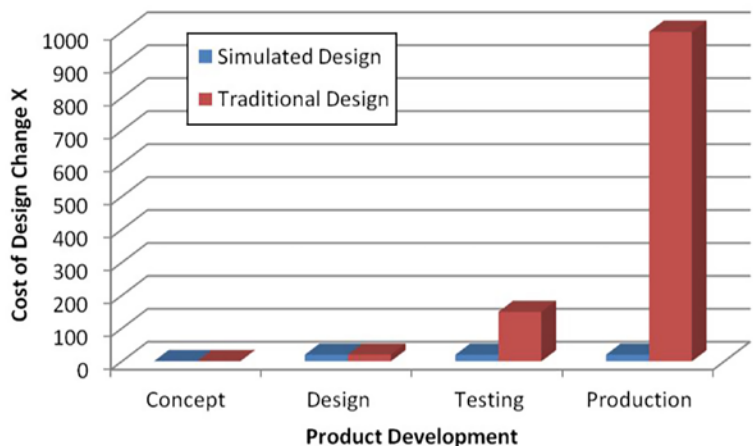


Figure 2: The cost of design change during product development. (Source: Mentor Graphics)

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Design changes that occur:

- In the conceptual stage cost nothing
- During the design stage requires just a little extra time
- During the test stage means that you have to regress one stage
- During production—or worse yet, in the field—can cost millions to fix and possibly damage the company’s reputation

Having the project completed on time and within budget means that costs are cut by reducing the design cycle and generating higher profits due to shorter time-to-market and an extended product life cycle.

The key to ensuring product reliability all begins in the design phase:

1. Controlling the impedance of single-ended and differential signals and matching the trace impedance to the driver prevents reflections, which cause crosstalk and electromagnetic emissions
2. Establishing design constraints based on simulation will ensure that the rules will be followed by downstream tools and validated to conform by the various design rule checkers (DRCs)
3. Providing a low AC impedance pat, for high current switching devices minimizes radiation from microstrip signals and from fringing fields of embedded stripline signals

A poorly designed substrate with inappropriately selected materials can degrade the electrical performance of the signal transmission, increasing emissions and crosstalk, and can also make the product more susceptible to external noise. These issues can cause intermit-

tent operation due to timing glitches and interference, dramatically reducing the product’s performance and long-term reliability.

Selecting the most suitable dielectric material for the substrate is one of the most important factors in establishing a reliable product. There are literally thousands of materials to choose from. However, when each material is used for the right target application, the resultant PCB will have the lowest possible cost while still satisfying the design and performance goals of the project. Selecting the best material for an application is often a daunting task, but armed with the right tools, one can quickly sort through the vast array of choices to make an informed decision.

The electrical properties of dielectric material can be described by two terms:

1. The dielectric constant (Dk), or relative permittivity (Er), is the ratio of the amount of electrical energy stored in a material by an applied voltage; it describes how the material increases the capacitance and decreases the speed in the material
2. The dielectric loss or dissipation factor (Df), or loss tangent ($\tan \delta$), is a parameter of a dielectric material that quantifies its inherent dissipation of electromagnetic energy

Figure 3 depicts the profile for dielectric materials with a $Df < 0.005$. The iCD Materials Planner has five default profiles ranging from basic FR-4 to ultra-low-loss materials as in Table 1. This enables the designer to compare dielectric materials based on the manufacturer, fabricator, frequency, dissipation factor (loss), and dielectric constant.

Profile	Bit Rate (Gbps)	Frequency (GHz)	Dissipation Factor (Df)
Ultra Low Loss	≥ 50	≥ 25	≤ 0.005
Low Loss	25–50	12.5–25	0.005–0.010
Mid Loss	10–25	5–12.5	0.010–0.015
Standard Loss	2–10	1–5	0.015–0.02
Basic FR-4	≤ 2	≤ 1	≥ 0.02

Table 1: Loss profile ranges.

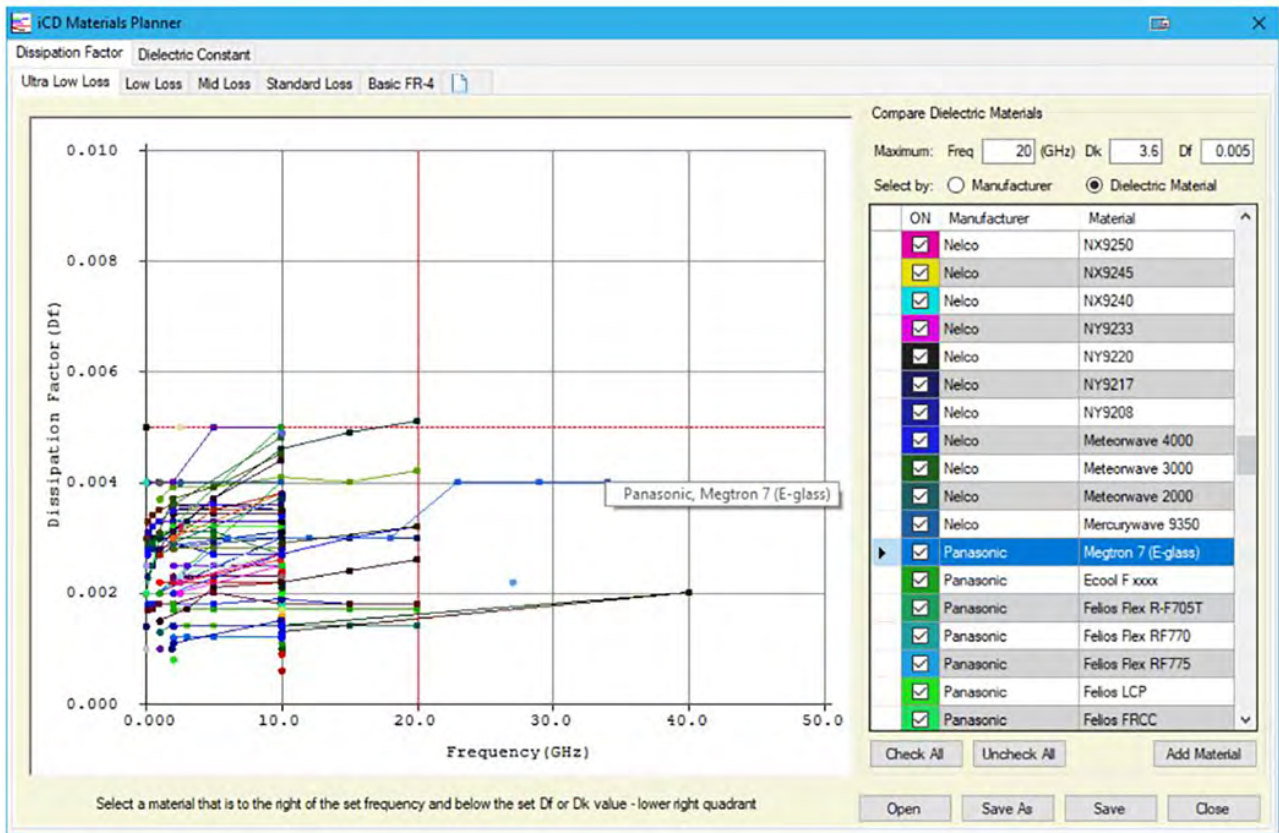


Figure 3: Loss profile for ultra-low-loss dielectric materials. (Source: iCD Materials Planner)

Differential Pairs > 50/100 Digital 40/80 DDR3 90 USB												
Layer No.	Via	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)
		Soldermask		PSR-4000 HFX Satin / CA-40 HF LPI ...	3.5	0.5						
1	8	Signal	Top	Conductive			2.2	12	4	0.43	51.67	98.65
		Prepreg		370HR ; 1080 ; Rc= 66% (1GHz)	3.97	2.9						
2		Plane	GND	Conductive			1.4					

Differential Pairs > 50/100 Digital 40/80 DDR3 90 USB												
Layer No.	Via	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)
		Soldermask		PSR-4000 HFX Satin / CA-40 HF LPI ...	3.5	0.5						
1	8	Signal	Top	Conductive			2.2	12	6	0.58	42.53	81.33
		Prepreg		370HR ; 1080 ; Rc= 66% (1GHz)	3.97	2.9						
2		Plane	GND	Conductive			1.4					

Differential Pairs > 50/100 Digital 40/80 DDR3 90 USB												
Layer No.	Via	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)
		Soldermask		PSR-4000 HFX Satin / CA-40 HF LPI ...	3.5	0.5						
1	8	Signal	Top	Conductive			2.2	6	4	0.43	51.67	90.63
		Prepreg		370HR ; 1080 ; Rc= 66% (1GHz)	3.97	2.9						
2		Plane	GND	Conductive			1.4					

Figure 4: Unlimited differential technologies can be defined on the same layer. (Source: iCD Stackup Planner)

Once the dielectric material has been selected, one needs to plan the most efficient stackup configuration for the design. For a typical digital design, 40–60 ohms impedance is recommended. However, numerous impedances are generally required to convey differential pairs of var-

ious technologies. Therefore, all combinations of impedances must be defined on the one substrate. Figure 4 shows three differential technologies defined on the same stackup layer.

Now that the stackup is finalized, let's look at impedance matching the source to the trans-

mission lines. The easiest way is to use a resistive element. Termination can be made at the source or at the load. Series termination is excellent for point-to-point routes (such as data signals)—one load per net. It works well for traces that are electrically short and is also used to fanout multiple loads radially from a common source whereas parallel termination, which has a resistance value equal to the transmission line impedance, is preferred for address buses.

The impedance of the trace is extremely important as any mismatch along the transmission path will result in a reduction in signal quality and possibly the radiation of noise. Mismatched impedance causes signals to reflect back and forth along the lines, which causes ringing at the load. This ringing reduces the dynamic range of the receiver, eats into the noise budget, and can cause false triggering.

In Figure 5, the attributes required to determine the source impedance of the driver are extracted from an IBIS model IV curves. Then, the required series termination resistance is calculated based on a distributed system to

match the transmission line for the selected layer in the iCD Stackup Planner.

The final attribute that determines the product's reliability is AC impedance of the power distribution network (PDN). One needs to ensure that the power planes and associated decoupling can handle the high switching current demanded by the processor and memory devices. Inadequate power delivery can exhibit intermittent signal integrity issues. These include high crosstalk and excessive emission of electromagnetic radiation, degrading the performance and reliability of the product. The PDN must accommodate variances of current transients with as little change in power supply voltages as possible. So, the goal of PDN planning is to design a stable power source for all of the required power supplies.

The same PDN connections (planes) used to transport high transient currents are also used to carry the return currents for critical signal transmission lines. If high-frequency switching noise exists between these planes, coupling may occur, resulting in ground (supply) bounce, bit failure, or timing errors. Many of the failures to pass electromagnetic compli-

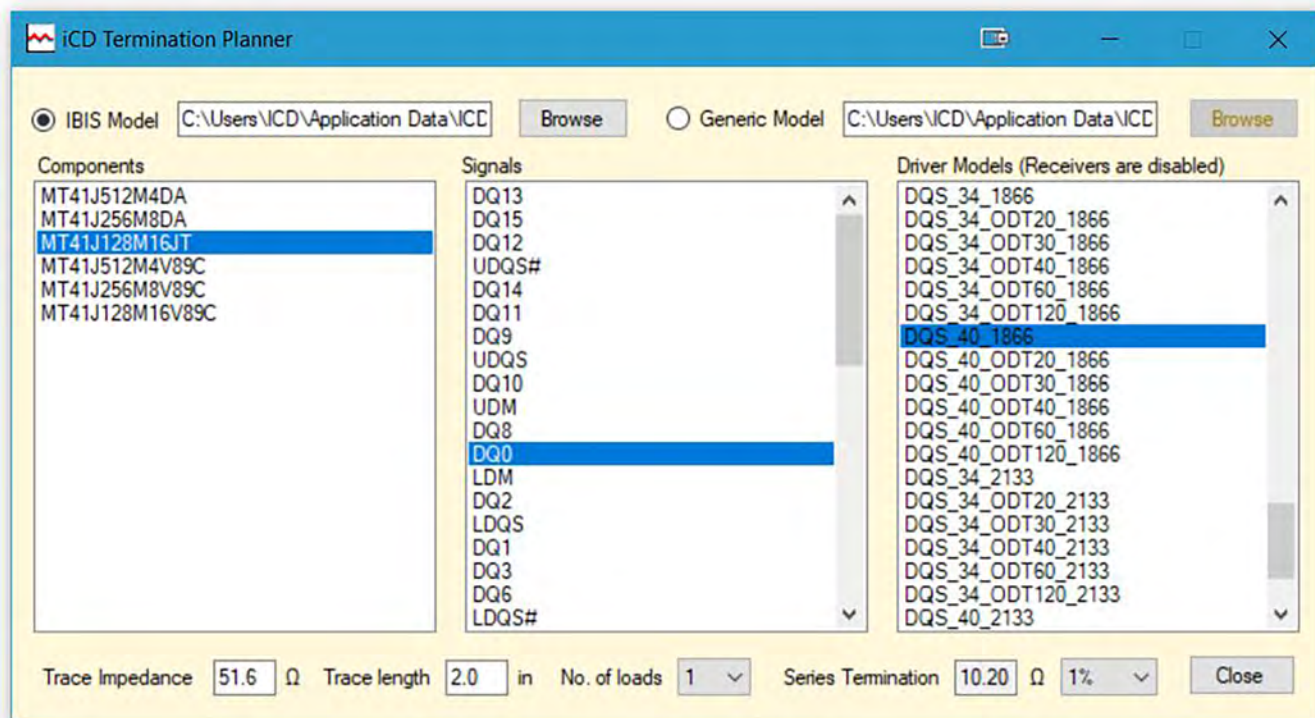


Figure 5: Series terminator extracted from the IBIS model. (Source: iCD Termination Planner)

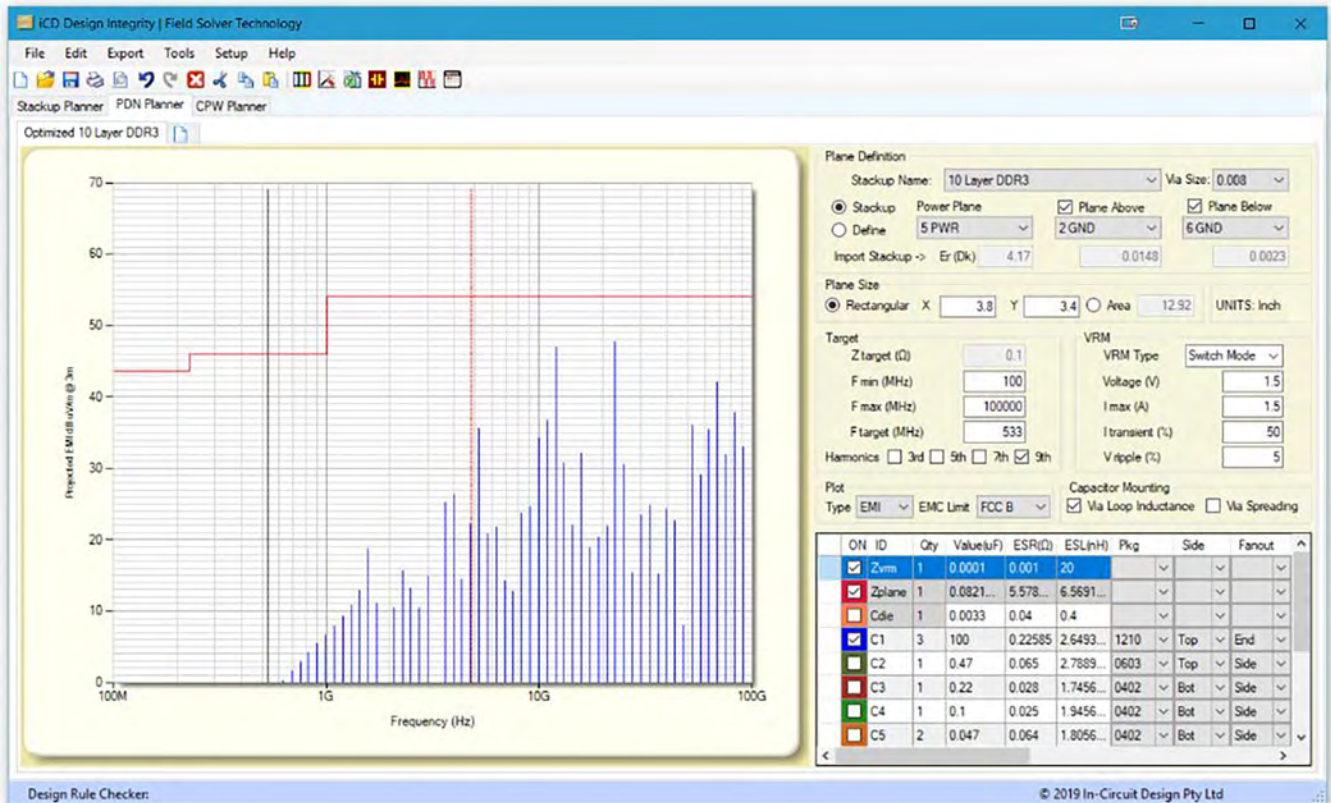


Figure 6: PDN noise between planes. (Source: iCD PDN Planner)

any (EMC) are due to excessive noise on the PDN coupling into external cables and radiating emissions. Figure 5 projects the radiation of the power planes relative to the FCC Class B limits. One also needs to ensure that the harmonics do not exceed the imposed limits.

The PDN is linked to the stackup; therefore, any adjustments to the stackup configuration—whether it be materials, vias, trace, clearance, or thickness parameters—should be reflected in the PDN. The PDN can be fine-tuned by adding more planar capacitance without affecting transmission line impedance. The optimization of the PDN is a trial-and-error process that needs to be done in conjunction with the stackup materials to fully exploit all avenues.

It is surprising how many designers do not get the basic key pillars of stability right. For very little extra effort, your design can have improved performance and reliability over a wide range of operating environments, giving you greater confidence in your product's performance for the projected lifetime.

Key Points

- Premature failures are of particular concern and are typically the result of poor design practice or substandard manufacture
- The cost of development is dramatically reduced if the simulation is employed early in the design cycle
- Simulation identifies issues early in the design process and rectifies them before they become a major problem
- The key to ensuring product reliability all begins in the design phase
- Selecting the most suitable dielectric material for the substrate is one of the most important factors in establishing a reliable product
- The electrical properties of dielectric material can be described by two terms: dielectric constant and dissipation factor
- The designer needs to compare dielectric materials based on the manufacturer, fabricator, frequency, dissipation factor (loss), and dielectric constant

- Numerous impedances are generally required to convey differential pairs of various technologies and must be defined on the one substrate
- The impedance of the trace is extremely important as any mismatch along the transmission path will result in a reduction in signal quality and possibly the radiation of noise
- Resistive terminations match the source to the transmission line
- Series termination is excellent for point-to-point routes whereas parallel termination is preferred for address buses
- One needs to ensure that the power planes and associated decoupling can handle the high switching current demanded by the processor and memory devices
- The goal of PDN planning is to design a stable power source for all the required power supplies
- Many of the failures to pass electromagnetic compliancy (EMC) are due to excessive noise on the PDN coupling into external cables and radiating emissions

Further Reading

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Barry Olney is managing director of In-Circuit Design Pty Ltd. (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded from www.icd.com.au. To read past columns or contact Olney, [click here](#).

AI-Driven Imaging System Protects Authenticity

Researchers at the NYU Tandon School of Engineering have demonstrated an experimental technique to authenticate images throughout the entire pipeline, from acquisition to delivery, using artificial intelligence (AI).

In tests, this prototype imaging pipeline increased the chances of detecting manipulation from approximately 45 percent to over 90 percent without sacrificing image quality.

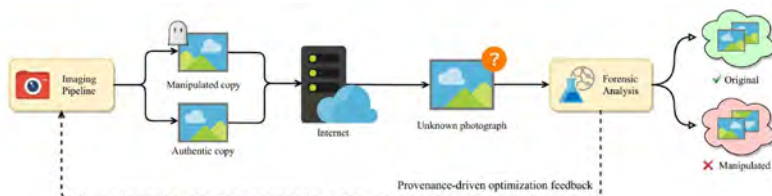
Determining whether a photo or video is authentic is becoming increasingly problematic. Sophisticated techniques for altering photos and videos have become so accessible that so-called "deep fakes"—manipulated photos or videos that are remarkably convincing and often include celebrities or political figures—have become commonplace.

Pawel Korus, a research assistant professor in the Department of Computer Science and Engineering at NYU Tandon, pioneered this approach. The process is optimized for in-camera embedding and can survive image distortion applied by online photo sharing services. The advantages of integrating such systems into cameras are clear.

"If the camera itself produces an image that is more sensitive to tampering, any adjustments will be detected with high probability," said Nasir Memon, a professor of computer science and engineering at NYU Tandon and co-author, with Korus, of a paper detailing the technique.

Korus and Memon, by contrast, reasoned that modern digital imaging already relies on machine learning. Every photo taken on a smartphone undergoes near-instantaneous processing to adjust for low light and to stabilize images, both of which take place courtesy of onboard AI.

(Source: NYU Tandon School of Engineering)

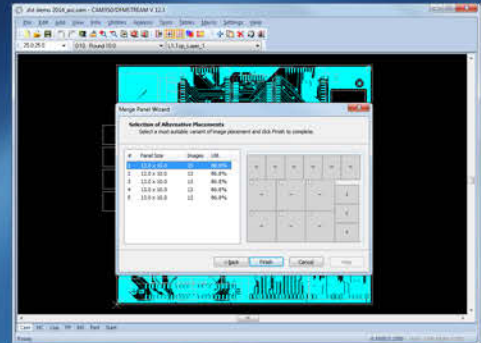


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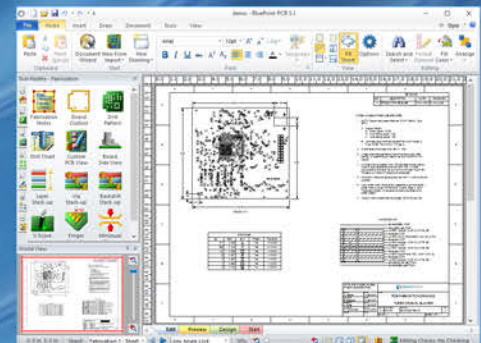
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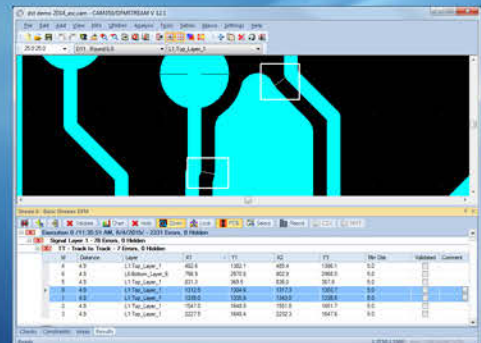
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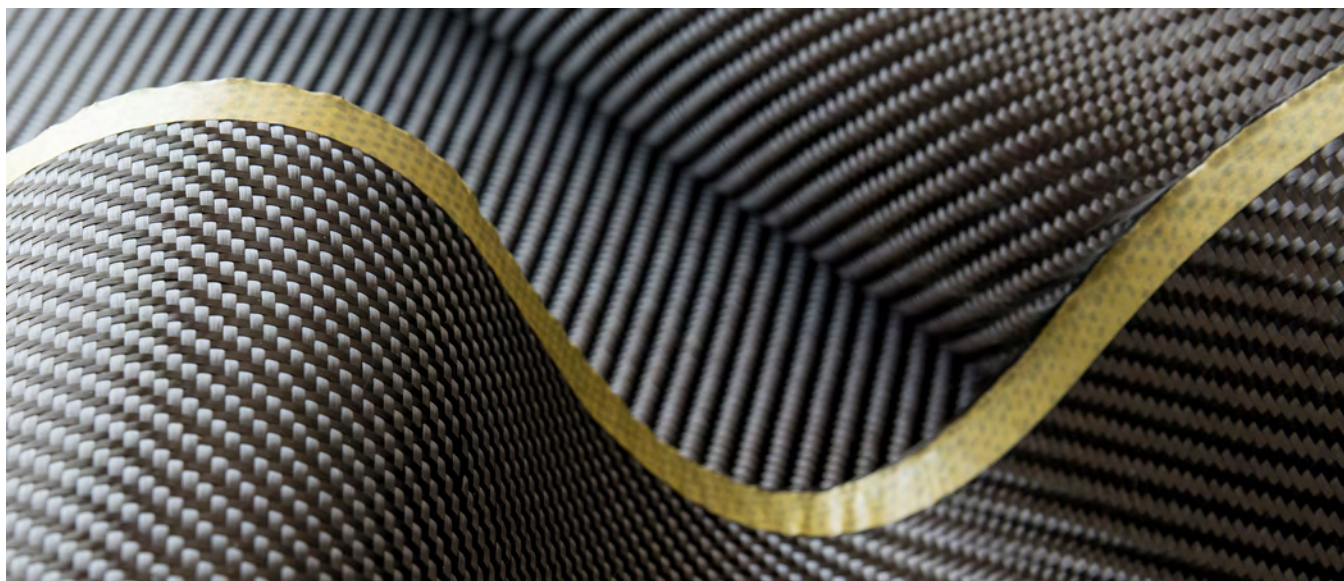
Practical Evaluations of Glass Weave Effect

Lightning Speed Laminates
by John Coonrod, ROGERS CORPORATION


The impact of glass weave effect on PCB electrical performance is a topic that has been investigated for many years. From my perspective, the initial investigators for the glass weave effect were mostly from the high-speed digital industry. However, as more RF applications are using millimeter-wave (mmWave) frequencies, the RF industry is now pursuing more studies for the potential of glass weave to impact these applications.

The basic issue for the glass weave effect is that many laminates have a layer, or layers, of woven fiberglass used to improve mechanical properties. The raw glass used to make the woven glass reinforcement layers is typically an E-glass, which has an approximate dielectric constant (Dk) of 6. As an example, for many laminates that have an overall Dk of 3.5, the resin system must have a much lower Dk than the glass, so the overall Dk of the laminate will be roughly 3.5.

For glass-reinforced laminates, and when looking down through the laminate, in isolated areas, the Dk of the laminate will be different in an area where there are glass bundles from the woven glass layer compared to areas where there are openings in the woven glass layer. In the open areas of the glass weave pattern, the Dk will be that of the resin system, and will probably have a Dk value around 2.1 to 3.0, depending on the laminate construction. In an area of the laminate where there is a combination of resin and one layer of glass bundles, the Dk will be somewhere between 2.1 and 6. In another area where the glass bundles intersect to form the grid of glass reinforcement, there will be two layers of glass as a knuckle and also the resin system. In these knuckle areas, the Dk will be the highest for the laminate. This means that within a small area of the laminate, there can be three areas of distinctly different Dk values.



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When a circuit pattern is adjacently aligned to the glass weave pattern within a laminate, there will be areas of very different Dk values. However, at low frequency or low-speed digital, these Dk differences blend together and give an average Dk value. This is typically not a problem for PCB electrical performance. However, at much higher frequencies, like mmWave and high-speed digital, the wave and the digital pulse can detect these Dk differences, which can alter the expected electrical performance of the circuit.

There are a few things to consider about the glass weave effect. One point of interest is when a laminate is using more than one layer of glass, the glass weave effect is somewhat dampened due to an averaging effect of the glass weave layers with their random alignment to each other. Another point of interest would be when a conductor is much larger than the geometry of the glass bundles, knuckles, and open area. Then, the conductor will experience an averaging of these different Dk

values from the glass weave effect. This is typically not a problem for electrical performance.

However, when the conductors are narrower than the glass bundles, knuckles, or open areas, and assuming higher frequencies or digital speeds, then the circuit can detect these Dk differences, and electrical performance of the circuit may be altered. In the last scenario, it is possible for one conductor to experience a different Dk value than a neighboring conductor on the same circuit, as shown in the left drawing in Figure 1.

There are two configurations where the glass weave effect can impact electrical performance; one is the locale trace environment and the other is the periodic Dk variation environment as shown in Figure 1. Rogers Corporation conducted a large study done last year to understand the glass weave effect, and it seems that the periodic Dk variation is probably more dominant than the local variation. However, in an effort to get a well-defined study, we purposely made circuits with con-

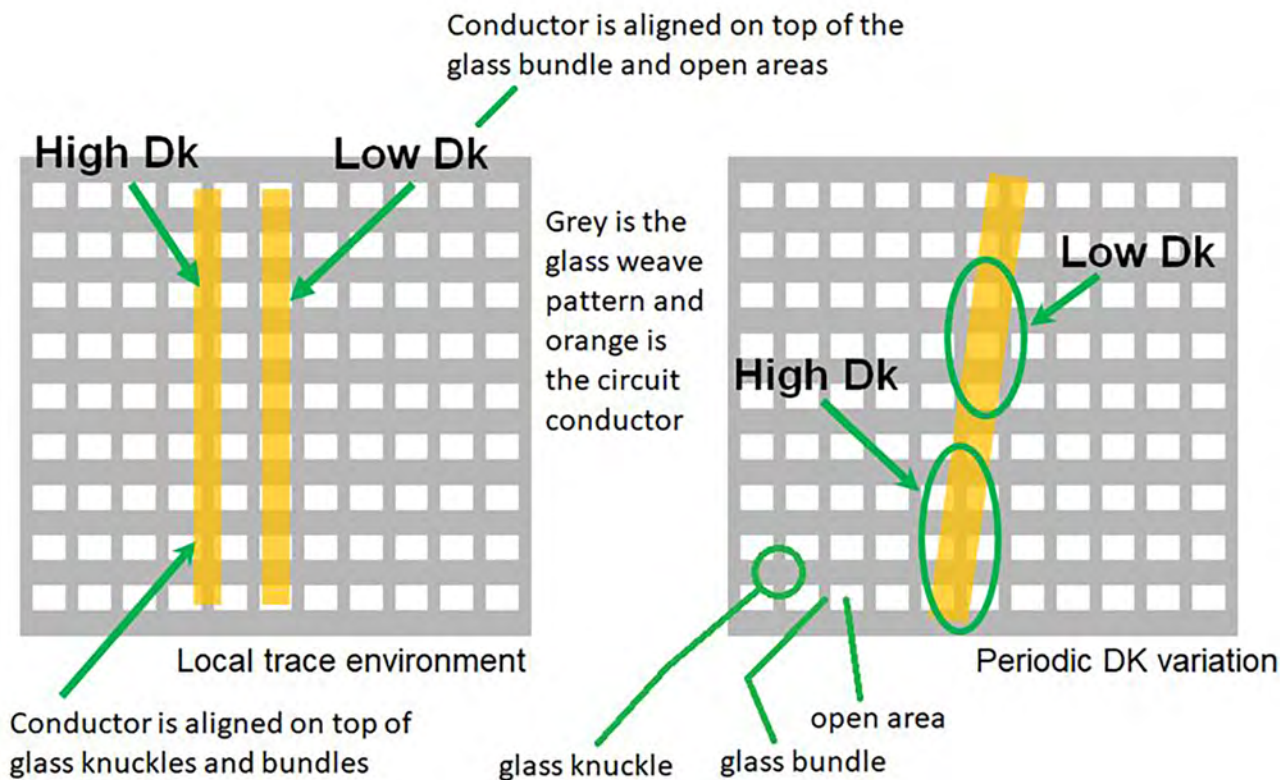


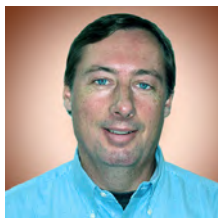
Figure 1: Top view of relationships between the glass weave pattern and circuit conductors, which can impact the Dk environment of the circuit.

ductors that were narrower than the glass weave geometry, and then inspected many circuits to evaluate which had the low and high Dk configuration from the local trace environment.

In this study, we used a worst-case scenario laminate, which was a pure resin system without any filler particles. Additionally, the laminate had one layer of glass reinforcement. From that study, and considering the low and high Dk from the local trace environment, we found a difference in Dk of 0.090 at 77 GHz when using 106 glass. When using 1080 glass, we saw a Dk difference of 0.14 at 77 GHz, and when using a spread glass (i.e., no openings in the glass-weave pattern), we saw a difference in Dk of 0.020 at 77 GHz.

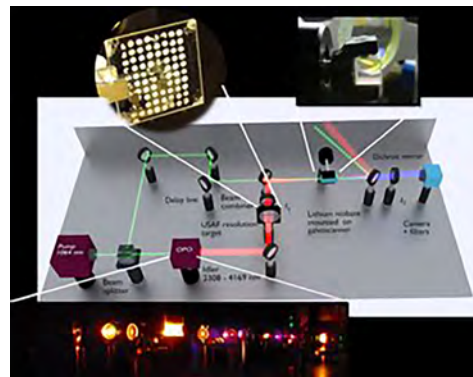
Also, as part of our glass weave study, we evaluated a ceramic-filled laminate using 1080 glass and compared the results to the unfilled laminate (as previously described) using the same glass style. Again, comparing the low and high Dk conductors as shown in Figure 1 for the local trace environment, we saw a Dk difference of 0.010 for circuits using 1080 glass with a ceramic-filled resin system. The same testing with the unfilled system mentioned earlier showed a Dk difference of 0.090. This shows that the ceramic particles used as filler in some laminates help to mitigate the glass weave effect.

Many available laminates do not contain woven glass, so the glass weave effect is not an issue. Some laminates intended to be used at mmWave frequencies do feature glass reinforcement; however, these laminates use a spread glass with ceramic filler. They are optimum for minimizing concerns of glass weave effect for mmWave and high-speed digital applications. **DESIGN007**



John Coonrod is technical marketing manager at Rogers Corporation. To read past columns or contact Coonrod, [click here](#).

New Approach Captures Detailed Mid-infrared Images for Medical Diagnostics



Researchers have developed a unique high-resolution imaging method that can capture mid-infrared spectral images of fast events or dynamic processes that take place on the order of milliseconds. This spectral range is used for many applications because it can reveal the detailed chemical composition of a sample.

"This novel approach could one day be used to pre-screen medical biopsies to identify the ones that need closer examination," said Peter Tidemand-Lichtenberg, a member of the research team from DTU Fotonik in Denmark.

The researchers drew on a process known as nonlinear frequency conversion in which energy is added to a photon to change its wavelength, and hence its color. Although frequency conversion, or upconversion, is often used to change the wavelength of a laser's output, the researchers from DTU Fotonik developed a detection system that could shift an entire mid-IR image into the near-infrared wavelength range while preserving all the spatial information.

The system incorporates a new mid-infrared light source developed by collaborators from The Institute of Photonic Sciences (ICFO). This single-wavelength light source can be tuned to different wavelengths and it also uses frequency conversion to generate the mid-infrared light. In fact, the researchers used the same pulsed near-infrared laser for two things: to generate the tunable mid-IR light and to achieve the image upconversion.

"This approach yields high peak power pulses in perfect synchronism, eliminating the need for sophisticated temporal control of the pulses, leading to images with a good signal-to-noise ratio," explained Tidemand-Lichtenberg. [Source: OSA]



MilAero007 Highlights



Incoming CEO Steve Pudles on the Acquisition of Zentech ▶

Nolan Johnson talks to Steve Pudles about the recent acquisition of Zentech Manufacturing Inc. by BlackBern Partners LLC and Zentech management. Steve, also an investor in Zentech, steps in as the incoming CEO of the new organization and discusses the deal, his new role, changes to management, and the company's plans post-sale.

Catching up With Darrel Yarbrough of YES ▶

Yarbrough Electronic Sales (YES) is one of the fastest growing contract manufacturers in the Southwest. As people get to know them better, they are becoming the go-to company in their area. In this interview, long-time industry veteran Darrel Yarbrough, owner of YES, provides a background about the company, its capabilities, and his outlook for the industry.

BAE Systems' Joint Strike Fighter Underpins Advanced Manufacturing Growth in South Australia ▶

BAE Systems Australia has celebrated the production of the 15,000th titanium part produced at Edinburgh Parks in South Australia for the world's largest defence program, the F-35 Joint Strike Fighter.

EPTE Newsletter: Global Electronics Industry Continue to Decline ▶

Sales from consumer electronics are expected to slip this year, continuing a decline that began in December 2018. The Taiwanese PCB industry was first to signal stormy days ahead, and data from the global semiconductor industry for the same month backed up this gloomy forecast.

IPC Releases Statement on New Tariffs on Chinese Goods ▶

Chris Mitchell, IPC Vice President for Global Government Relations, has released the following statement in line with the Office of the U.S. Trade Representative's announcement that it will begin formal procedures to impose a fourth round of tariffs against China.

Saab to Open U.S. Site for Advanced Manufacturing ▶

Saab announces a new site for advanced manufacturing and production in West Lafayette, Indiana, USA. Located at the Purdue University-affiliated Discovery Park District.

NA PCB Industry Book-to-Bill Ratio Retreated to 1.00 for March ▶

Total North American PCB shipments in March 2019 were up 19.1% compared to the same month last year. Year-to-date sales growth as of March was 16.4%. Compared to the preceding month, March shipments jumped 32.9%.

Green Circuits' Three Tips to Be a Well-prepared Customer ▶

Nolan Johnson speaks with Joe Garcia, VP of sales and marketing at Green Circuits, about how they can help on both the front and back end of the process, their hidden gem—design services—as well as three tips to be a well-prepared customer.

Top 7 U.S. Aerospace and Defense Companies ▶

Global defense spending has been on a steady upswing since the past couple of years with the same reaching the \$1.8 trillion mark for 2018, the highest level since the post cold war low of 1998.



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Stitching Capacitor: Crosstalk Mitigation for Return Path Discontinuity

Article by Chang Fei Yee
KEYSIGHT TECHNOLOGIES

This article discusses the impact of stitching capacitors ^[1] in mitigating signal crosstalk due to return path discontinuity during layer transition on PCB. The investigation was performed with 3DEM simulation using Keysight EMPro.

Introduction

In electronic systems, signal transmission exists in a closed-loop form. The forward current propagates from transmitter to receiver through the signal trace. On the contrary, the return current travels backward from receiver to transmitter through the power or ground plane right underneath the signal trace that serves as the reference or return path. The path of the forward current and return current forms a loop inductance. It is important to route the high-speed signal on a continuous reference plane so that the return current can propagate on the desired path, directly beneath the signal trace.

When the return path is broken due to the switching of reference planes with different

potential, (e.g., from ground to power or vice versa after layer transition on PCB), the return current might detour and propagate on a longer path, which causes a rise in loop inductance. This might lead to the sharing of a common return path by different signals that pose a high risk of interference among the signals due to higher mutual inductance. This interference results in signal crosstalk. To mitigate the crosstalk due to return path discontinuity (RPD), stitching capacitors are mounted on the PCB to serve as a bridge between the two reference planes of interest on different PCB layers.

Analysis of Signal Crosstalk

To investigate the impact of stitching capacitor in mitigating signal crosstalk due to RPD during layer transition on PCB, three simulation models of 3DEM are constructed. In model 1A (Figure 1), two signal traces with 50 ohm characteristic impedance in single-ended mode on the top PCB layer transition to the bottom layer using vias. Each segment of the signal traces on top and bottom layers is 100 mils long and 5 mils wide. Meanwhile, the diameters of the via barrel and pad are 5 mils and 7 mils respectively.

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The PCB stackup shown in Figure 2 is applied to this 3D model, where solid planes exist on layer 2 and 3. All the four copper layers are 1.2 mils thick and FR-4 material is used as the PCB substrate.

The two signal traces are 15 mils apart, which is triple the signal trace width for minimum crosstalk due to forward current propagation. A stitching via is placed 20 mils off each signal via, connected to the reference plane on layer 2 and extending to layer 4. However, voids are placed on the layer 3 reference plane to break the electrical connectivity between the planes on layer 2 and 3. This simulates the effect of RPD on signal crosstalk by switching the reference from ground to power or vice versa after the signal layer transition through the via.

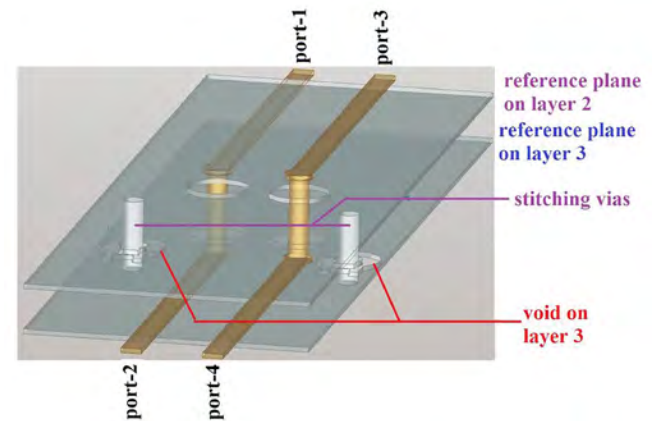


Figure 1: 3DEM structure in model 1A.

	thickness (mils)
solder mask top	0.5
signal L1	1.2
substrate	3.5
plane L2	1.2
substrate	10
plane L3	1.2
substrate	3.5
signal L4	1.2
solder mask bottom	0.5

Figure 2: The PCB stackup discussed here.

From a crosstalk perspective, port 1 and port 2 terminations refer to the transmitting and receiving ends, respectively, of the aggressor line. On the other hand, port 3 and port 4 terminations refer to the transmitting and receiving ends, respectively, of the victim line.

In model 1B (Figure 3), a stitching capacitor is inserted into the void on the right side (i.e., highlighted in red) to electrically connect the reference plane on layer 3 and the stitching via extending from the reference plane on layer 2. The rest of the portion is the same as model 1A. This ideal 0.1uF capacitor, without parasitic resistance (ESR) and parasitic inductance (ESL) [2] serves as a single return path in transmission line.

On the other hand, in model 1C depicted in Figure 4, one more ideal 0.1uF stitching capacitor is inserted into the void on the left side, highlighted in red, to electrically connect the

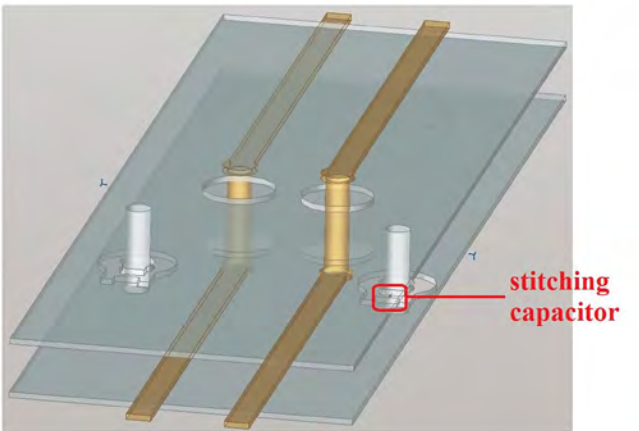


Figure 3: The 3DEM structure in model 1B.

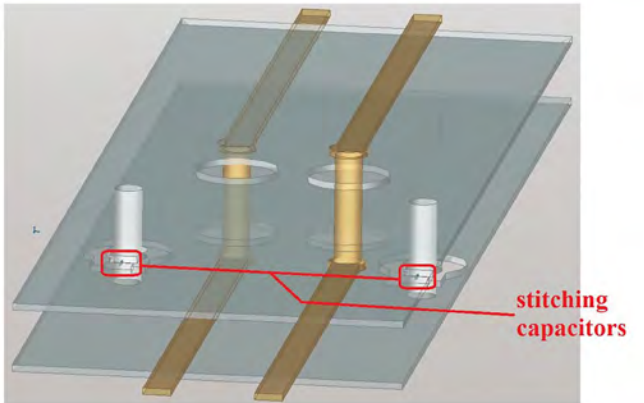


Figure 4: The 3DEM structure in model 1C.

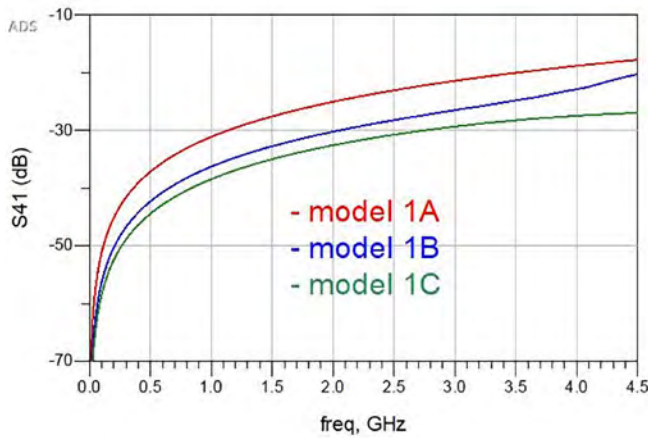


Figure 5: S41 plots for model 1A, 1B and 1C.

reference plane on layer 3 and the stitching via extending from the reference plane on layer 2. These two capacitors provide two return paths in the transmission line.

The S41 parameter or far-end crosstalk (FEXT) of these 3DEM models are plotted in Figure 5 (i.e., the span from 1MHz to 4.5GHz).

A more severe crosstalk is indicated by a smaller absolute value in dB. With reference to Figure 5, the most severe signal crosstalk is experienced by model 1A, followed by 1B, with the least severe by 1C. Model 1A suffers from total RPD. Alleviation of crosstalk due to RPD is achieved by providing more return paths using capacitors to bridge the reference planes on layer 2 and 3.

Subsequently, transient simulation is performed for these three models to observe the phenomenon of FEXT in time domain. In this transient simulation, a square wave signal with 1Gbps data rate (500MHz Nyquist frequency), 1.5Vpp amplitude and 5V/ns slew rate is injected into port 1 of each model's 3DEM model, with port 3 being pulled low (serving as the near-end point of the victim line), followed by probing at port 4 (serving as the far-end point of the victim line). Referring to Figure 6, noise induced at the far-end point of the victim line in time domain

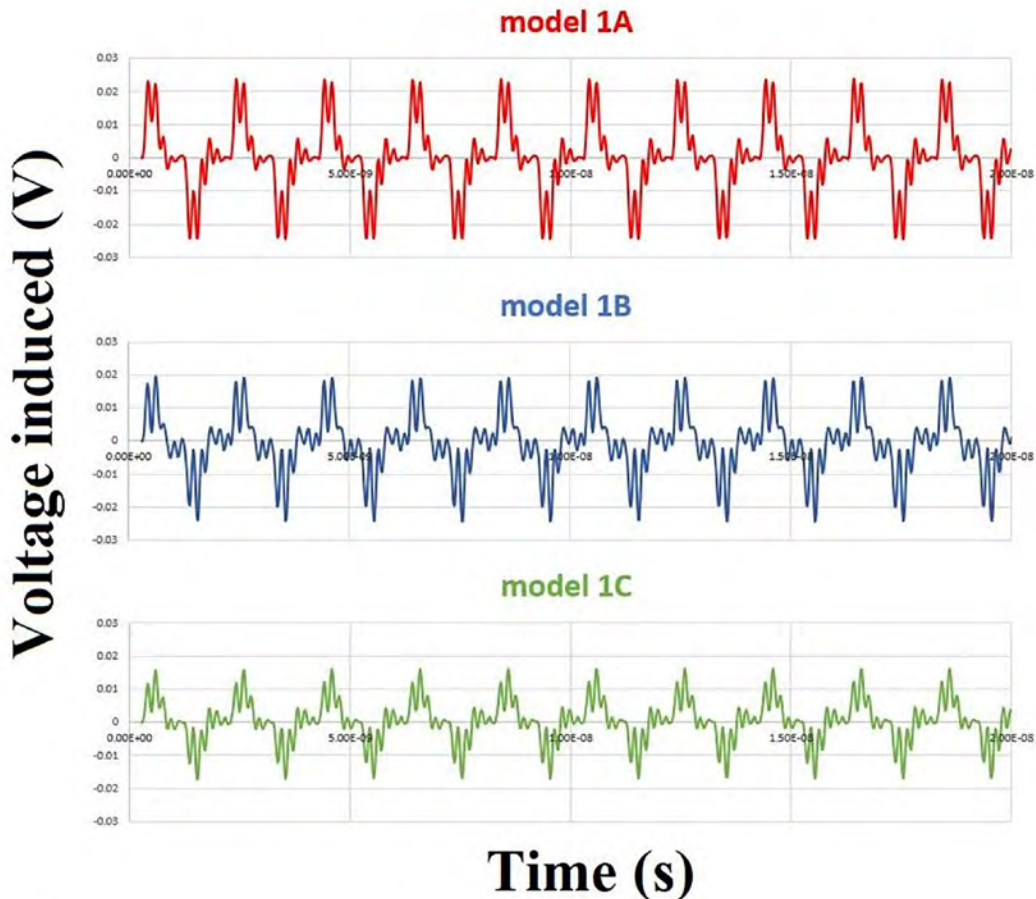


Figure 6: Noise induced at far-end point of victim trace for three models due to crosstalk.

for model 1A, 1B and 1C is 50mVpp, 45mVpp and 30mVpp respectively.

The smallest amplitude of noise is induced at far-end point of victim line in model 1C due to the least crosstalk incurred, contributed by more return paths provided by the additional stitching capacitor, versus the single return path with only one stitching capacitor in model 1B and total RPD (i.e., without a stitching capacitor) in model 1A.

The study is further carried out to analyze the effect of ESR and ESL on mitigating the crosstalk due to RPD. Practically, a discrete capacitor has intrinsic parasitic ESR and ESL in series with it, depicted in Figure 7. The 3DEM simulation is repeated on model 1C, but varying the value of ESR and ESL in the two stitching capacitors respectively. With reference to

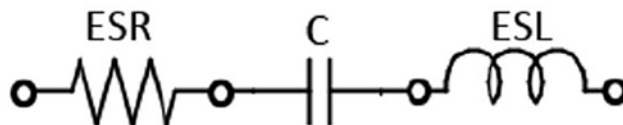


Figure 7: Simplified model of practical capacitor with ESR and ESL.

S41 plots in Figure 8, ESR of 0.15ohm worsens the FEXT by 0.075dB at a frequency near 500MHz. Similarly, with reference to S41 plots in Figure 9, ESL of 0.5nH intensifies the FEXT by 1.5dB at frequency near 500MHz. A further increase of ESL to 2nH contributes an additional 0.4dB to FEXT.

In fact, the ESR and ESL are directly proportional to the impedance of the stitching capacitor. A larger impedance in the stitching ca-

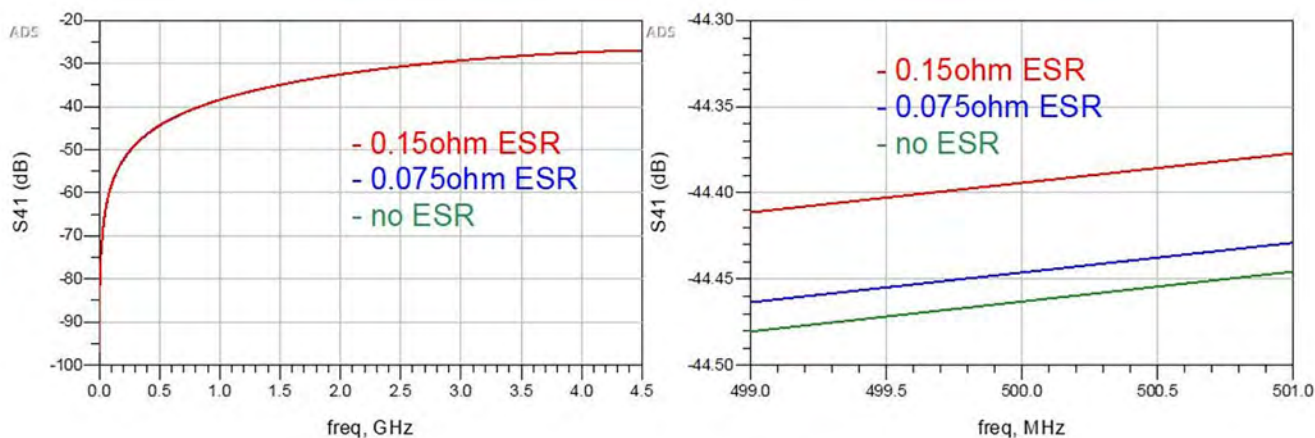


Figure 8: S41 plots for model 1C with effect of ESR at full frequency span (left) versus zoomed in (right).

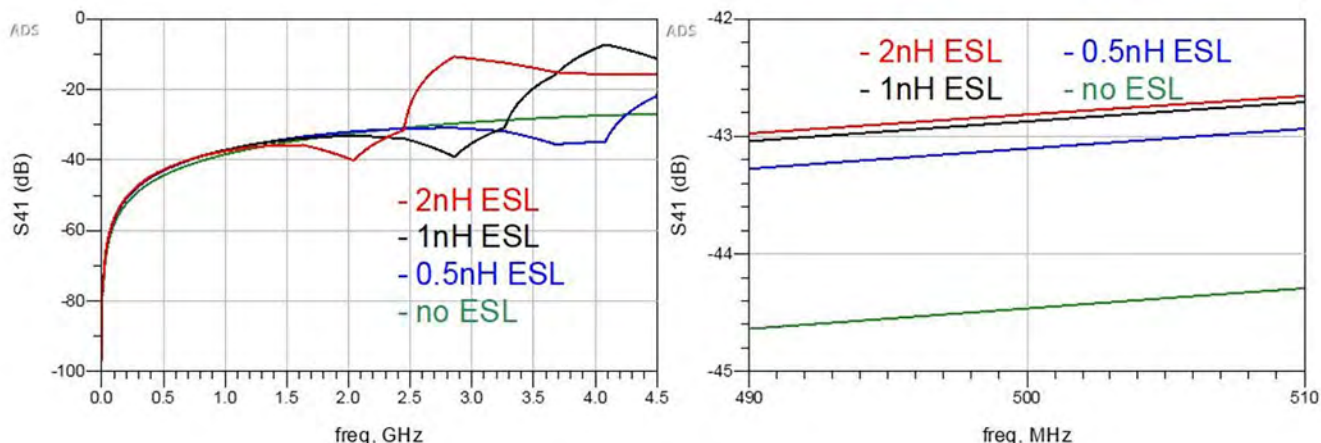


Figure 9: S41 plots for model 1C with effect of ESL at full frequency span (left) versus zoomed in (right).

pacitor due to larger ESR and ESL contributes to higher resistance in the signal return path, which in turn intensifies the FEXT.

Summary

It is crucial to provide a continuous return path for high-speed signaling during layer transitions to minimize signal crosstalk. Crosstalk due to RPD caused by switching of reference planes with different potential during signal layer transition is reduced by as much as 10dB after bridging by the stitching capacitors. Moreover, a stitching capacitor with smaller ESR and ESL can provide a low-

impedance signal return path to achieve minimal crosstalk. **DESIGN007**

References

1. *Stitching Capacitors*, by Kenneth Wyatt
2. *What is the ESR/ESL of capacitors?* Taiyo Yuden



Chang Fei Yee is a hardware engineer with Keysight Technologies. His responsibilities include embedded system hardware development, and signal and power integrity analysis.

Radar Sensor Module to Bring Added Safety to Autonomous Driving

When a child runs out onto the road, the average human driver takes 1.6 seconds to hit the brake pedal. The reaction time is cut to 0.5 seconds for automated vehicles fitted with radar/lidar sensors and a camera system. But at a speed of 50 km/h, that still means that the vehicle will continue for another seven meters before the brakes are applied and it comes to a standstill.

The Fraunhofer Institute for Reliability and Microintegration IZM has teamed up with a range of partners to develop a camera radar module that is significantly faster in capturing changes in traffic conditions. The new unit, no bigger than a smartphone, will have a reaction time

of less than 10 milliseconds, which, according to a study conducted by the University of Michigan, makes it 50 times faster than current sensor systems and 160 times faster than the average human driver.

The real innovation in the new system is its integrated signal processing capacity. This allows for processing to take place directly within the module, with the system selectively filtering data from the radar system and stereo camera so that processing can either take place immediately or else be intentionally delayed until a subsequent processing stage.

As a result, the system has no need to send status information to the vehicle, but solely reaction instructions. "Integrated signal processing drastically cuts down reaction times," says Christian Tschoban, group head in the RF & Smart Sensor Systems department.

Tschoban is currently working on the KameRad project. The functioning demonstrator he and his team have developed looks like a grey box with eyes to the right and left: the stereo cameras. Tschoban hopes that in a few years his "grey box" will be fitted as standard in every vehicle.

(Source: University of Michigan)



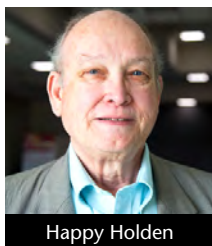


1 The Shaughnessy Report: Get Smart! ▶

It sounds so perfect—"smart" manufacturing. That must be what we've needed all along! We've had enough of this "average intelligence" manufacturing. Yes, we've heard quite a bit of chatter about smart manufacturing over the past few years. Whatever "smart" means to you, everyone involved in designing, fabricating, and assembling PCBs wants to get on board.

2 Automation and the Smart Factory: Introduction to Industry 4.0 ▶

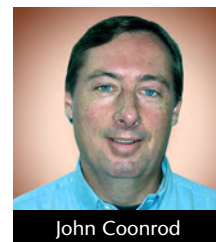
There's a lot of talk about automation, but I find that there is very little available on automation planning. This is one of my specialties. I started by studying for an MSEE in control theory, which went well with my bachelor's degree in chemical engineering because I specialized in process control and IC manufacturing.



Happy Holden

3 Lightning Speed Laminates: How Copper Properties Impact PCB RF and High-speed Digital Performance ▶

The circuit is a microstrip with a signal conductor on the top copper plane and a ground plane on the bottom of the circuit. Additionally, the concept of skin depth and wave propagation should be considered. Skin depth is the depth within the cross-sectional area of the copper where the majority of the RF current resides and is dependent on frequency.



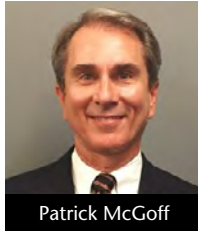
John Coonrod

4 iCD Releases Impedance Goal-seeking Functionality ▶

In-Circuit Design Pty Ltd (iCD), Australia has released a new target Impedance Goal Seeking Algorithm to add to the Stackup Planner functionality. This release will be rolled out to all iCD support customers as an update to their current software.

5 Smart Design Data Is Essential for Industry 4.0 Manufacturing ►

Almost all of the conversation regarding Industry 4.0 is centered on the manufacturing floor, which is where the effect of the initiative is most felt initially. Little attention is given to the starting data for manufacturing—the data that comes from design. However, you can't have smart manufacturing if your process begins with dumb data.

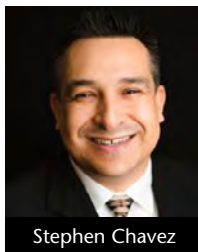


6 Learning to Be More Flexible: Case Studies on Improving FPC Design ►

As miniaturization requirements force manufacturers to pack more functionality into ever-smaller packages, it becomes more difficult to conform to IPC construction recommendations. Achieving robust FPCs requires frequent, iterative interaction internally among the mechanical, electrical, and PCB design teams, as well as with the fabricators and assemblers.

7 The Digital Layout: San Diego Chapter Updates and More ►

This month's column is packed with recent activities, including a spotlight on the San Diego Chapter and an interview with Luke Hausherr, the new chapter president. You'll also find an update from the IPC Designers Council Executive Board as collaboration with the new IPC Education Foundation continues to evolve and recommended reading featuring an interview with a young designer.



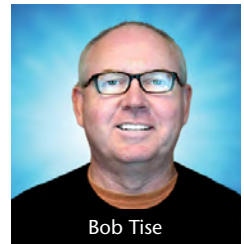
8 EM Modeling: The Impact of Copper Ground Pour on Loss and Impedance ►

This article briefly introduces the general purposes of copper ground pour on printed circuit boards. Subsequently, the impact of copper ground pour on PCB channel loss in terms of insertion loss and impedance in terms of time domain reflectometry (TDR) is studied with electromagnetic modeling using Mentor HyperLynx.



9 Connect the Dots: Preparing for Tomorrow's Technology Today ►

At a recent Sunstone Circuits planning summit, Matt Stevenson, VP of sales and marketing, and I led a wide-ranging discussion about emerging technologies and how they will impact PCB manufacturing. The following is an abridged transcript of this conversation.



10 Pulsonix 10.5 PCB Design Tools Get New 3D Capabilities, Constraint Rules ►

Pulsonix has released Pulsonix version 10.5, with over 30 new enhancements based on user requests from professional PCB designers.



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Insulectro, the largest national distributor of printed circuit board materials, is seeking a talented sales superstar for a Technical Account Manager role based out of either our Chicago or Minneapolis office. This role will focus on maintaining the existing customer base and developing new business within the assigned territory in both the printed circuit board and printed electronics industries. We are looking for the perfect fit of education, experience, and attitude that matches our company culture and enhances the service level to our customers.

Qualifications:

- A self-motivated business professional who is driven to succeed with a minimum of 3 years outside sales experience in the PCB or PE industry
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- Excellent communication and interpersonal skills
- OEM and electronic assembly experience is a plus

We offer:

- Competitive salary and commission plan with a comprehensive benefits package
- A fun, high-energy company with an entrepreneurial spirit
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We believe in caring about our people because they are our greatest asset. CML works with multicultural stakeholders daily to achieve more and bring them the best solutions. That's why we continuously invest in optimizing our culture and focus on providing our team with opportunities to develop their skills (e.g., through professional coaching to achieve their highest potential).

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In addition, this post will participate in system development projects and provide support including, but not limited to, user requirement collection and analysis, user training, system documentation, system support and maintenance, enhancement, and programming.

- Develop and enhance related IT systems and applications
- Prepare functional specifications
- Transfer the relevant business and interface processes into IT systems and other applications to get a maximum automation degree and prepare all required business reports
- Conduct function testing and prepare documentation
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APCT, Printed Circuit Board Solutions: Opportunities Await

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APCT currently has opportunities in Santa Clara, CA; Orange County, CA; Anaheim, CA; Wallingford, CT; and Austin, TX. Positions available range from manufacturing to quality control, sales, and finance.

We invite you to read about APCT at APCT.com and encourage you to understand our core values of passion, commitment, and trust. If you can embrace these principles and what they entail, then you may be a great match to join our team! Peruse the opportunities by clicking the link below.

Thank you, and we look forward to hearing from you soon.

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Technical Service Engineer (PCB Process Engineer) Plano, Texas

PRIMARY FUNCTION:

To provide expert technical advice on production and engineering issues in the application of solder mask and other Taiyo products.

ESSENTIAL DUTIES:

- Troubleshoot customer problems
- Conduct technical audits
- Advise and consult on product evaluations
- Conduct technical presentations
- Frequent travel to customer facilities (travel required, up to 50% of the time)
- Write trip/audit reports
- Coordinate travel arrangements to realize significant transportation savings
- Respond to and write email messages
- Write monthly reports
- Prepare agendas for customers, detailing goals and objectives
- Must comply with all OSHA and company workplace safety requirements at all times

OTHER DUTIES:

- Other duties as assigned from time to time

REQUIRED EDUCATION/EXPERIENCE:

- College degree preferred with solid knowledge of chemistry
- 10 years of technical work experience in the printed circuit board (PCB) industry
- Computer knowledge
- Good interpersonal relationship skills

WORKING CONDITIONS:

- Occasional weekend or overtime work

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Field Service Engineer: Multiple U.S. Locations

Reporting to a regional service manager, these customer-focused engineers will uphold the Koh Young culture while delivering professional technical services for our award-winning portfolio of inspection solutions. The role will enthusiastically visit our growing list of customers for installations, training, and evaluations, as well as technical support and maintenance.

We are looking for candidates with a technical degree or equivalent plus three or more years in a production environment with relevant experience. Given our growing customer base, the position will require extensive travel, including some internationally, as well as a collaborative attitude that drives success.

Koh Young is the leading 3D measurement-based inspection equipment and solutions provider. We perform quality control and process optimization across a growing set of industries including PCBA, machining, final assembly, process manufacturing, and semiconductors. In addition to our corporate office in Seoul, our international sales and support offices help us maintain a close relationship with our customers and provide access to a vast network of inspection experts.

Join the industry's leading provider of true 3D inspection solutions. Forward your resume to Michelle.Hayes@KohYoung.com.

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Vision and Machine Learning R&D Engineer Atlanta, GA or San Diego, CA

At Koh Young, we are focused on developing the future and continue to bolster our newly established R&D center near San Diego, California, with top talent focused on vision engineering and machine learning for electronics and medical applications. Currently, we are collaborating with top medical universities and hospitals across the U.S., Korea, and Japan to develop innovative neurosurgical robotic systems. With core technologies developed in-house, we expect to deliver neurosurgical breakthroughs.

The role will develop practical, scalable 3D machine learning solutions to solve complex challenges that detect, recognize, classify, and track medical imagery. Additional focus on the design, implementation, and deployment of full-stack computer vision and machine learning solutions.

The ideal candidates will hold a master's (doctorate preferred) in computer science or electrical engineering with at least three years of relevant experience. We desire a strong understanding of machine learning and computer vision algorithm application within embedded systems, plus significant vision expertise in multi-view geometry, 3D vision, SFM/SAM, and activity recognition.

Koh Young is the leading 3D measurement-based inspection solutions provider. We perform quality control and process optimization across a growing set of industries including electronics, final assembly, semiconductors, and most recently, medical imagery.

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- Marketing and sales
- Finance and accounting
- Machine operators and production
- Research and development
- Operations

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THERMAL SYSTEMS

Service Engineer Reflow Soldering Systems (m/f)

To strengthen our service team at Rehm Thermal Systems LLC. in Roswell, Georgia, we are seeking candidates to fill the position of Service Engineer—Reflow Soldering Systems.

Your area of responsibility:

- Installation of Rehm reflow soldering systems at the customers' site
- Maintenance and repair work as well as technical service for our customers in the USA and Mexico
- Execution of machine training

Your profile:

- Completed education studies as an engineer in the field of electrical engineering/mechatronics or comparable education (m/f)
- Basic and specialist knowledge in the field of electronics and electrical engineering/mechatronics
- High willingness to travel and have flexible employment
- Service-oriented and like to work independently

We offer:

- Performance-oriented, attractive compensation
- Comprehensive training
- A safe workplace in one successful group of companies
- Self-responsibility and leeway

Please send application documents online to Natalie Werner at n.werner@rehm-group.com.

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Career Opportunities



SMT Operator Huntingdon Valley, PA

Manncorp, a leader in the electronics assembly industry, is looking for a technician to operate our new in-house SMT LED assembly lines.

Duties and Responsibilities:

- Set up and operate automated SMT assembly equipment
- Prepare component kits for manufacturing
- Perform visual inspection of SMT assembly
- Participate in directing the expansion and further development of our SMT capabilities

Requirements and Qualifications:

- Prior experience with SMT equipment, or equivalent technical degree preferred
- Basic computer knowledge
- Proven strong mechanical and electrical troubleshooting skills
- Experience programming machinery or demonstrated willingness to learn
- Positive self-starter attitude with a good work ethic
- Ability to work with minimal supervision

We Offer:

- Paid training period
- Health and dental insurance
- Retirement fund matching
- Continuing training

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SMT Field Technician Huntingdon Valley, PA

Manncorp, a leader in the electronics assembly industry, is looking for an additional SMT Field Technician to join our existing East Coast team and install and support our wide array of SMT equipment.

Duties and Responsibilities:

- Manage on-site equipment installation and customer training
- Provide post-installation service and support, including troubleshooting and diagnosing technical problems by phone, email, or on-site visit
- Assist with demonstrations of equipment to potential customers
- Build and maintain positive relationships with customers
- Participate in the ongoing development and improvement of both our machines and the customer experience we offer

Requirements and Qualifications:

- Prior experience with SMT equipment, or equivalent technical degree
- Proven strong mechanical and electrical troubleshooting skills
- Proficiency in reading and verifying electrical, pneumatic, and mechanical schematics/drawings
- Travel and overnight stays
- Ability to arrange and schedule service trips

We Offer:

- Health and dental insurance
- Retirement fund matching
- Continuing training as the industry develops

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Career Opportunities



Sales Personnel, Japan

The Gardien Group is looking to expand the sales team in Tokyo, Japan, and seeking highly motivated team players with a positive attitude. Prior experience in the PCB industry is an advantage but not necessary for the right candidate.

The role involves working closely with the customer to identify their needs and deliver the right solution. The candidate should be able to offer a high level of customer satisfaction to ensure ongoing sales.

Training will be provided along with a competitive benefits package, excellent growth opportunities, and periodic bonuses.

Interested candidates, please contact us at careers.jp@gardien.com with your resume.

Kindly note only shortlisted candidates will be notified.

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Sales Representatives (Specific Territories)

Escondido-based printed circuit fabricator U.S. Circuit is looking to hire sales representatives in the following territories:

- Florida
- Denver
- Washington
- Los Angeles

Experience:

- Candidates must have previous PCB sales experience.

Compensation:

- 7% commission

Contact Mike Fariba for more information.

mfariba@uscircuit.com

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The successful candidate will benefit from a generous package and report directly to the U.S. general manager.

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Zentech is an IPC Trusted Source QML and ITAR registered. U.S. citizens only need apply.

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IPC Master Instructor

This position is responsible for IPC and skill-based instruction and certification at the training center as well as training events as assigned by company's sales/operations VP. This position may be part-time, full-time, and/or an independent contractor, depending upon the demand and the individual's situation. Must have the ability to work with little or no supervision and make appropriate and professional decisions. Candidate must have the ability to collaborate with the client managers to continually enhance the training program. Position is responsible for validating the program value and its overall success. Candidate will be trained/certified and recognized by IPC as a Master Instructor. Position requires the input and management of the training records. Will require some travel to client's facilities and other training centers.

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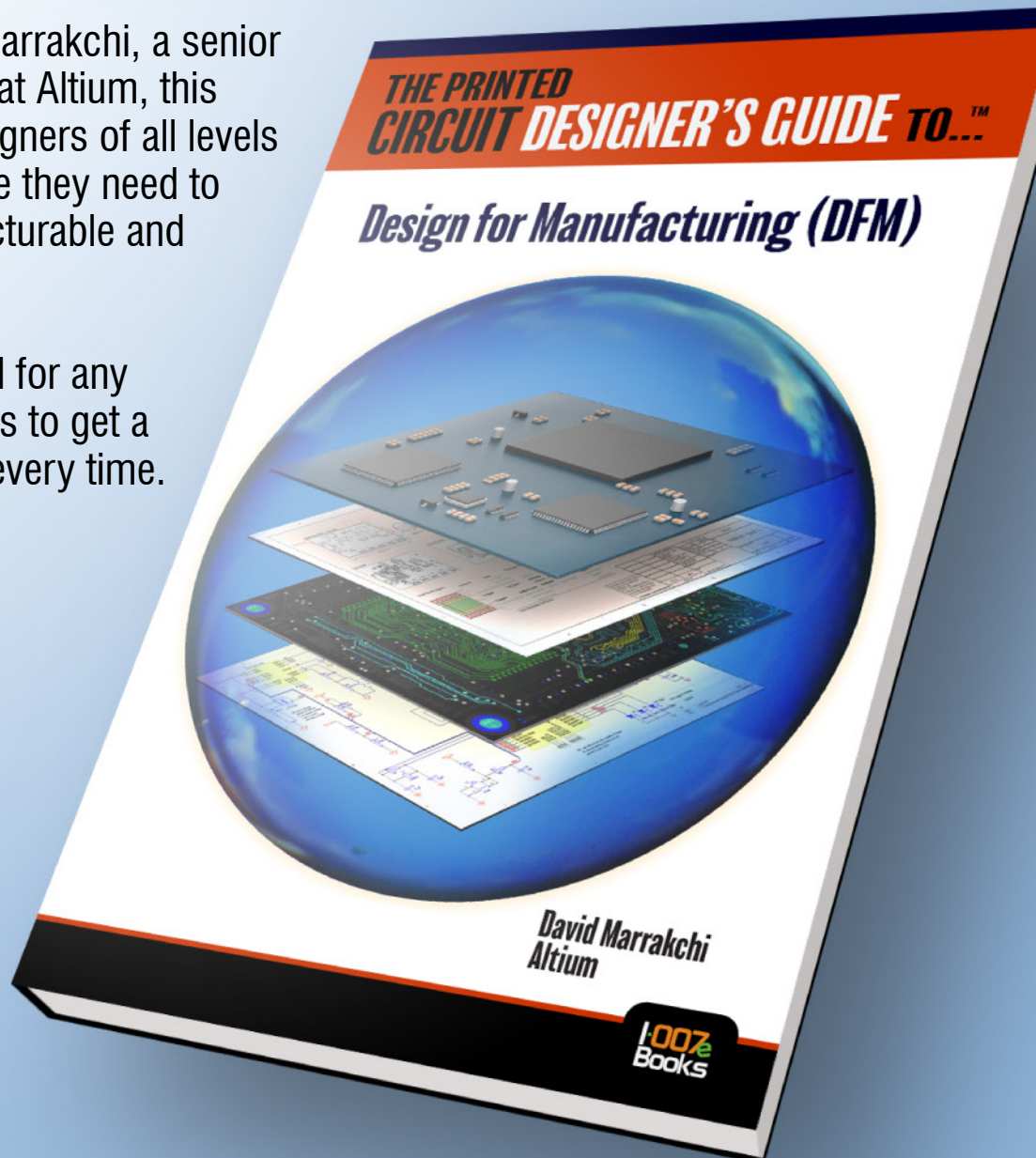
CID+, CIT, EPTAC Corporation

Written by David Marrakchi, a senior technical engineer at Altium, this book provides designers of all levels the DFM knowledge they need to produce a manufacturable and functional board.

This is a must-read for any designer who wants to get a good board back, every time.



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June 11–13, 2019
New York, New York, USA

EIPC Summer Conference 2019 ▶

June 13–14, 2019
Leoben, Austria

IPC SummerCom ▶

June 15–20, 2019
Raleigh, North Carolina, USA

NEPCON Thailand 2019 ▶

June 19–22, 2019
Bangkok, Thailand

Embedded Technologies Expo & Conference ▶

June 25–27, 2019
San Jose, California, USA

NEPCON South China 2019 ▶

August 28–30, 2019
Shenzhen, China

PCB West 2019 ▶

September 9–11, 2019
Santa Clara, California, USA

SMTA International 2019 ▶

September 22–26, 2019
Rosemont, Illinois, USA

productronica and electronica India 2019 ▶

September 25–27, 2019
Delhi NCR, India

52nd International Symposium on Microelectronics ▶

September 29–October 3, 2019
Boston, Massachusetts, USA

productronica 2019 ▶

November 12–15, 2019
Munich, Germany

Additional Event Calendars



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